Picosecond Photodetectors: What can we learn from modern III-V semiconductor technologies?

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Outline

- CNSE brief overview
- Applications of ps UV photodetectors
- Vertical vs. Lateral field PDs
- Fast APDs
- How to make ps single-photoelectron counting detector?
- III-V technologies – challenges and breakthroughs
- Summary

CNSE OVERVIEW

Mr. Ross Goodman, Esq.
Assistant Vice President, Business Development and Economic Outreach
SUNY College of Nanoscale Science and Engineering

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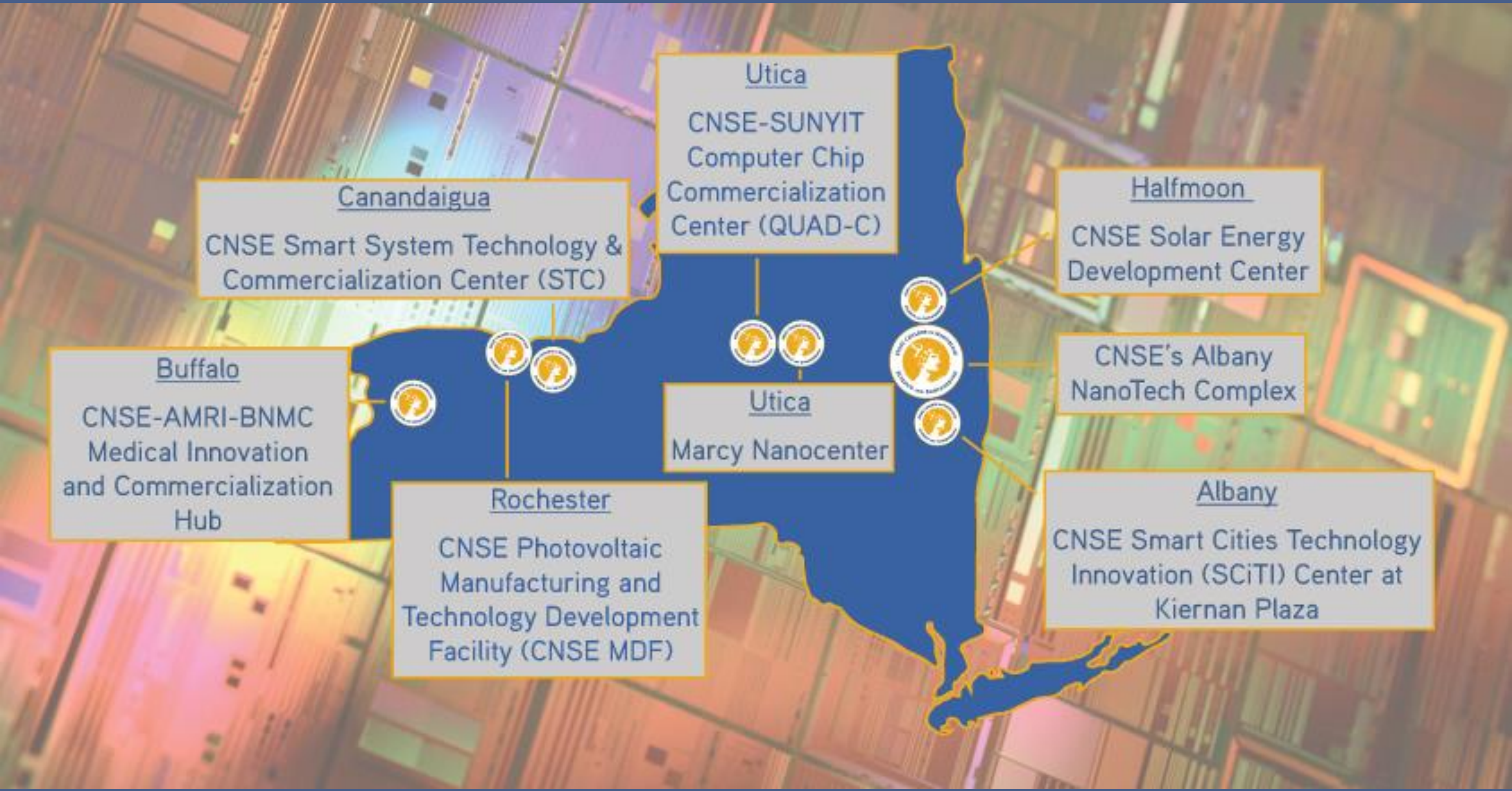
World Class Facilities

- > 1,000,000 sq.ft. of cutting-edge facilities, with 135,000 sq. ft. of 300mm and 450 mm cleanrooms with a current expansion to 1,300,000 sq. ft.
- More than 300 industry partners including electronics, energy, defense & biohealth
- Over $17B investments and over 3,100 R&D jobs currently on site

CNSE's STATEWIDE NANO IMPACT



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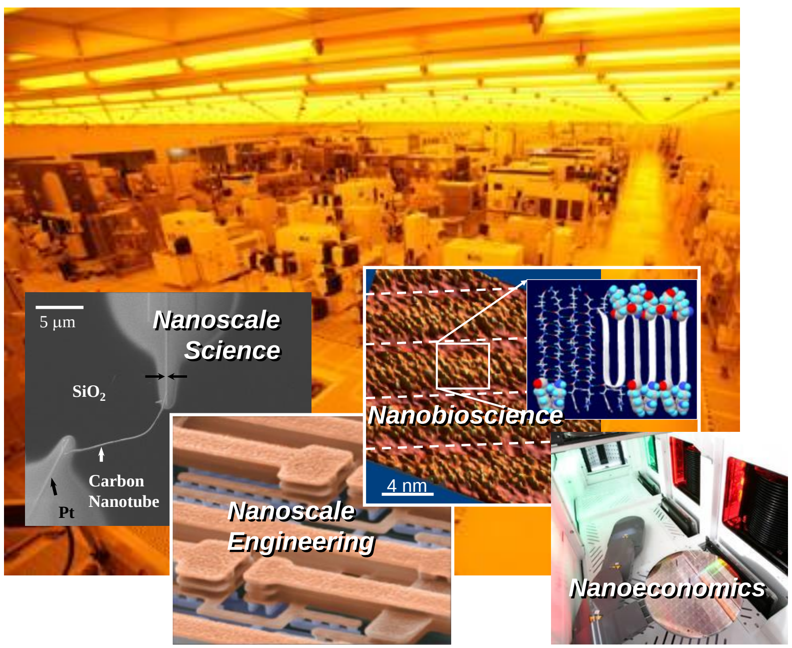
Cross-Disciplinary Mission

CNSE is dedicated to nanotechnology with constellations in:

- **Nanoscience**
- **Nanoengineering**
- **Nanobioscience**
- **Nanoeconomics**

Vision Leverage combined resources to establish effective partnerships that will enable <u>realization of *industry* technology roadmaps</u> and pioneering nanoscale research.

Mission Create a financially and technically competitive environment to <u>empower the nanoelectronics *industry*</u> with manufacturing advantages through vertically integrated partnerships.



NYS Governor Cuomo Announces Global 450 Consortia

- $4.8 billion investment
  - $4.4 billion pledged by IBM, Intel, TSMC, GlobalFoundries, Samsung
  - $400 million pledged by NYS
- Intel to establish its East Coast headquarters in Albany to manage 450mm development.

  R&D in Albany, Canandaigua, Utica, East Fishkill and Yorktown Heights.

  2,700 new high-tech jobs, including:
  - 800 at the CNSE
  - 400 in Utica
  - 1,500 construction jobs in Albany

CNSE Site Expansion

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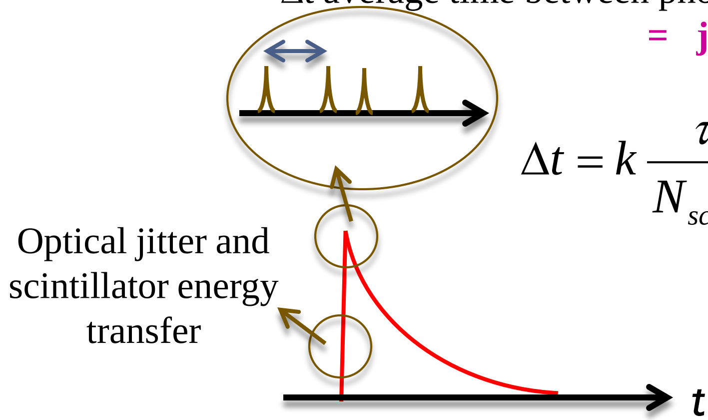
Picosecond near UV Semiconductor Photodetectors : Applications

Applications for ultra-fast UV photodetectors:

- High energy physics
  - LAr and LXe detectors
  - Fast crystal calorimetry: many inorganic scintillators, i.e. BaF_2, emit in UV
  - Cherenkov detectors
- Space research
- Medical TOF imaging and tomography
  - TOF positron emission tomography
  - Fast gamma imaging/ TOF tomography

Scintillator emission

Δt average time between photons = **jitter**



$$\Delta t = k \frac{\tau_{sc}}{N_{sc} K_{eff}}$$

K_{eff} – system collection efficiency
τ_{sc} – scintillator decay time
N_{sc} - scintillator photon yield
k~1 coefficient close to unity (statistics dependent)

Example: Projected time resolution for TOF PET

	Decay time (ns)	Light output (ph./MeV)	Δt at K_{eff}=0.2 & 0.5 MeV (ps)
LYSO	40	40,000	10
BaF_2 (fast component)	0.9	1400	6
$LaBr_3$ (Ce)	16	70,000	3
CsBr	0.07	20	35

Need: Semiconductor UV/Vis single photoelectron detector with ps resolution

Materials: Bulk Properties

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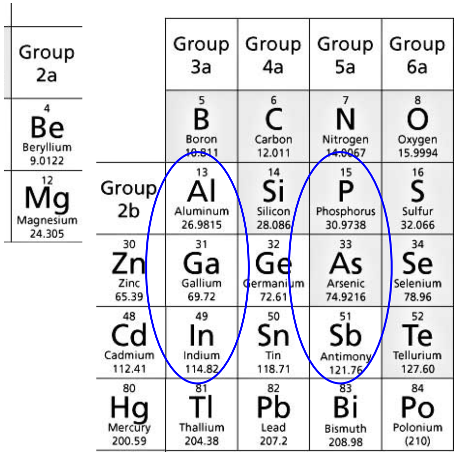
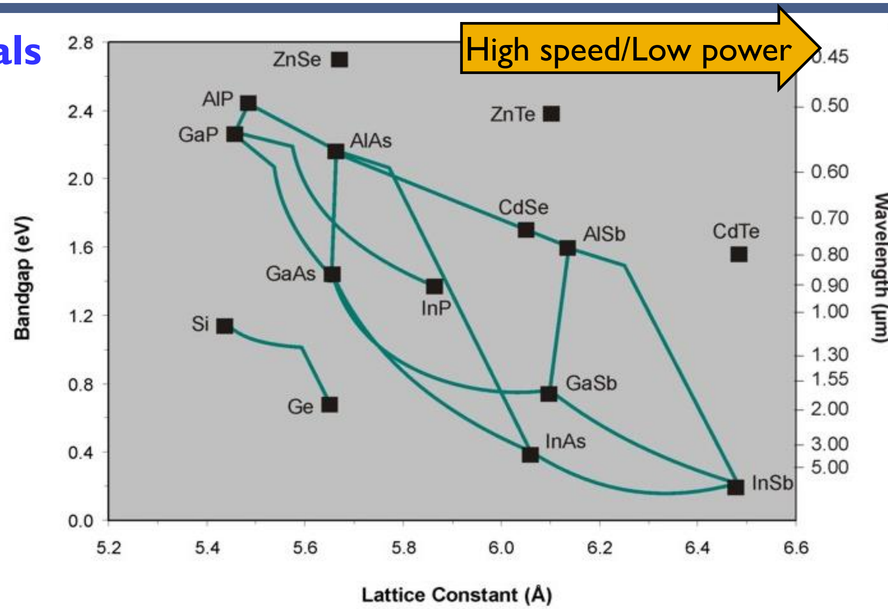
Group III-V materials





Attractive material parameters are similar for MOSFETs and ultrafast PDs

300 K Electron Transport Properties / 300 K Hole Transport Properties

	E_g, eV	$m_{e(-t)}$	$m_{e-(l)}$	μ_e, cm^2/Vs	$V_{e,sat}$, 10^7cm/s	m_{hh}	m_{lh}	$m_{hh\text{-}in\_pl}$	μ_h, cm^2/Vs
Si	1.12	0.19	0.98	1350	0.7	0.54	0.15	0.22	460
Ge	0.66	0.082	1.64	3900	0.7	0.34	0.043	0.057	1900
GaAs	1.42	0.067	-	8500	2	0.53	0.08	0.11	400
InP	1.35	0.079	-	5900	2.4	0.56	0.12	0.16	150
$In_{0.53}GaAs$	0.8	0.04	-	14000	2.9	0.36	0.041	0.052	400
InAs	0.36	0.027	-	33000	3.5	0.4	0.026	0.035	450
GaSb	0.73	0.041	-	3750		0.8	0.05	0.055	680
InSb	0.17	0.013	-	77000	5.0	0.42	0.016	0.020	850

Materials: Saturation Velocity

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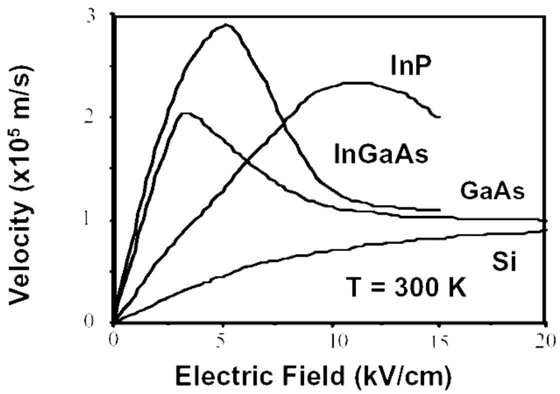
Drift velocity

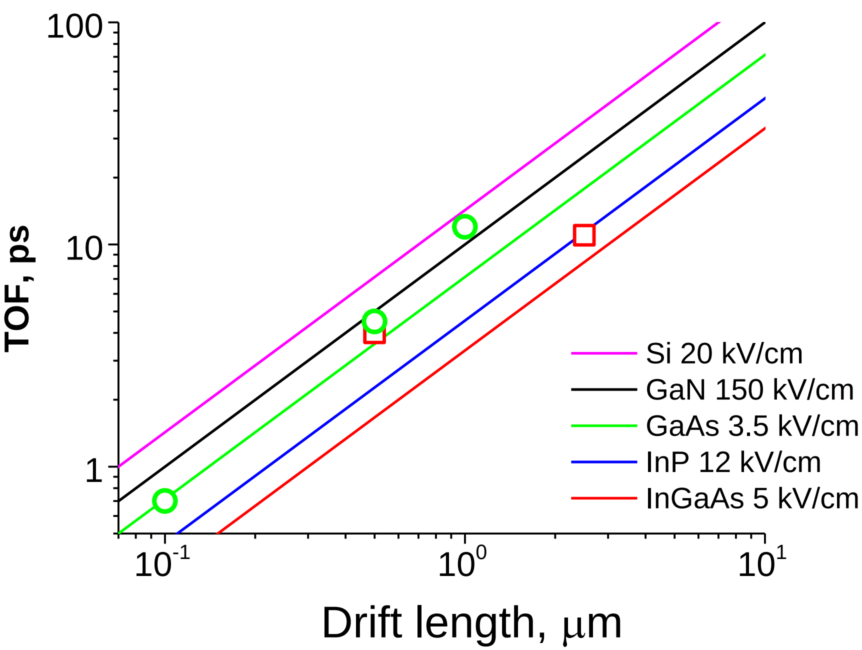


Saturation velocity and necessary operating voltage for 10ps risetime

Material	Saturation field, kV/cm	Spacing for 10ps, μm	Operating Voltage, V
Si	20	0.7	1.4
GaN	150	1.4	21*
GaAs	3.5	2	0.7
InP	12	2.3	2.6
InGaAs	5	3	1.5

* For GaN operating voltage should be further increased due to longer absorption lengths and lower mobility

Saturation velocity – limited electron drift time (TOF)

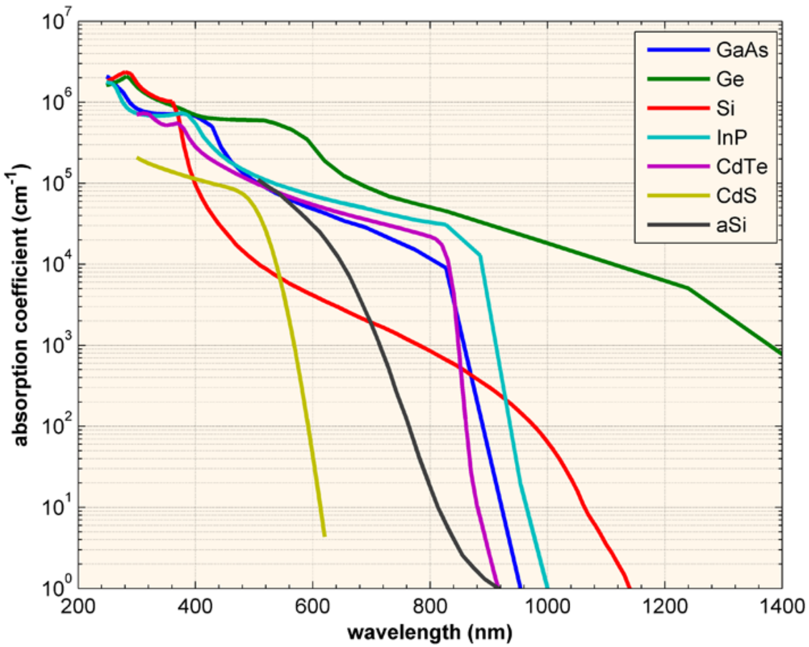


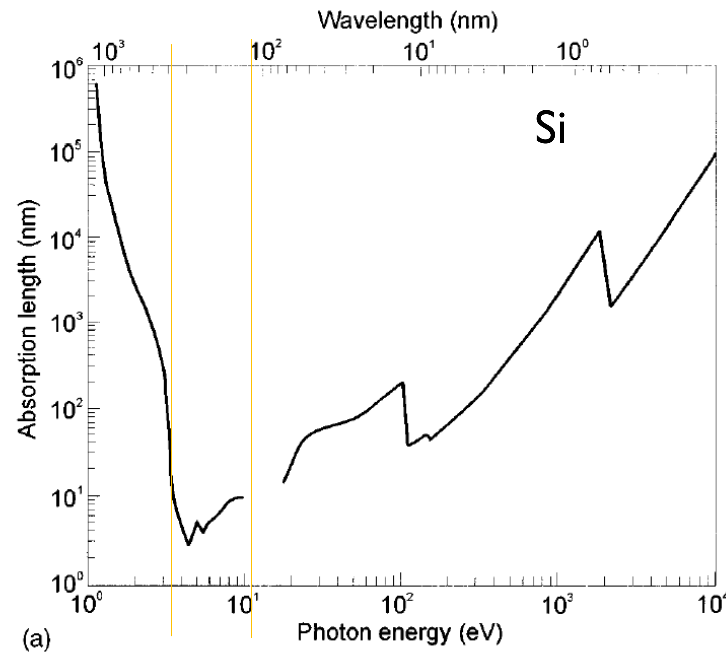
Experimental data from:
III-V MSMs (lateral field): Ralph 1992, Zeghbroeck 1988, Chou 1992, Gallo 2013,

Absorption

Absorption coefficients in semiconductors

[Carruthers, Electro-Optics Handbook]



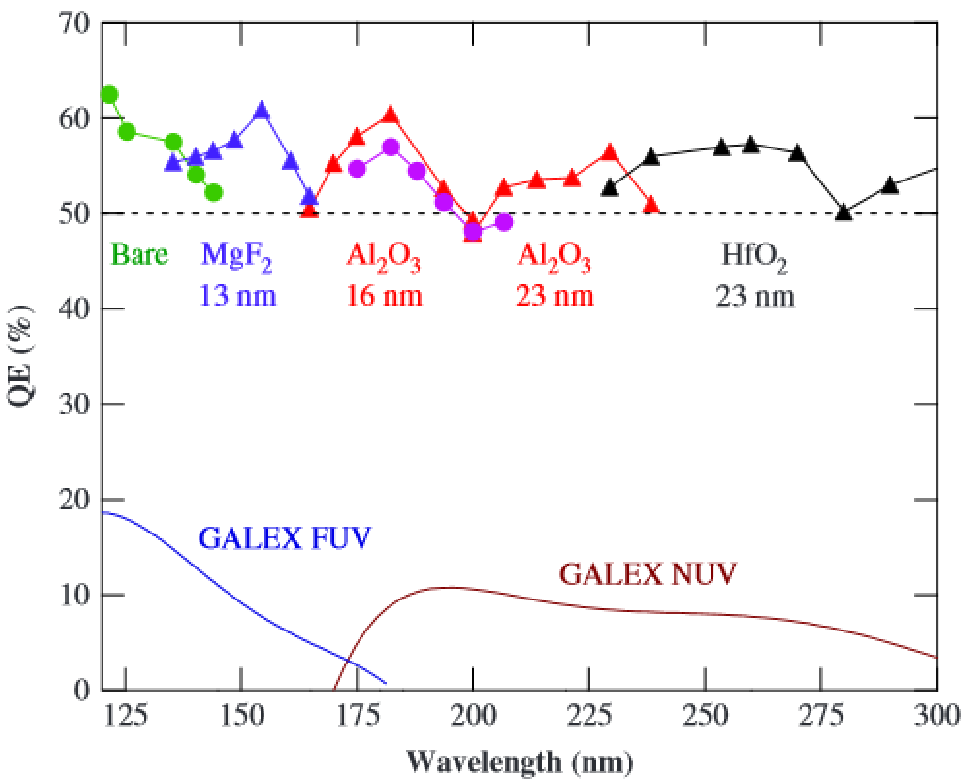


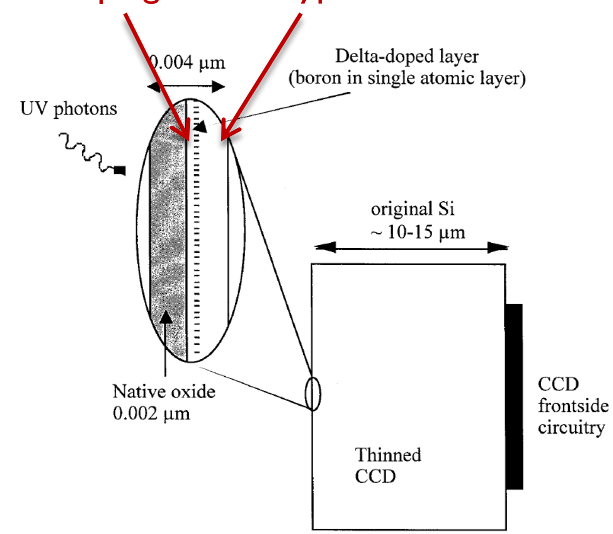
- **In the region λ<360nm the absorption takes place within <100 A**
- **Highly-doped layer in p-i-n or APD structures kills efficiency**
- **Evolution of carriers is strongly affected by the surface/interface recombination, relaxation in the Brillouin zone close to the surface**
- **Si has the highest α in UV and the lowest in visible → the worst material for fast PDs**
- **Detectors with lateral field are of great interest for (near)-UV**

UV QE Enhancement in Si

Quantum efficiency of UV-enhanced (delta-doped) CCDs 4x4 μm^2 pixel [JPL]

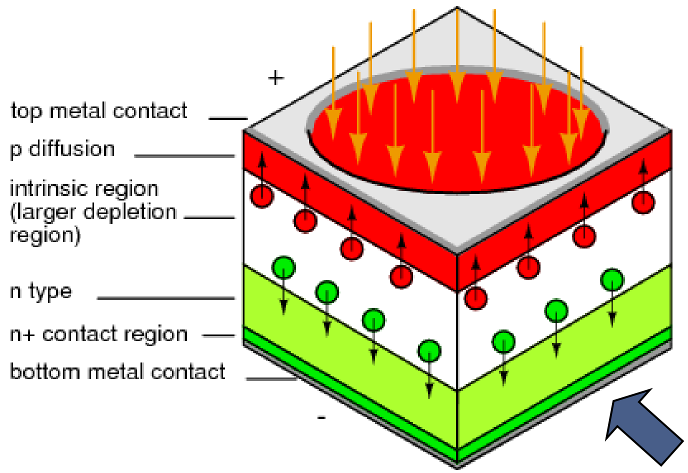
Nikzad et al. Appl. Optics **51** 365(2012); Proc. SPIE **2198** 907 (1994).



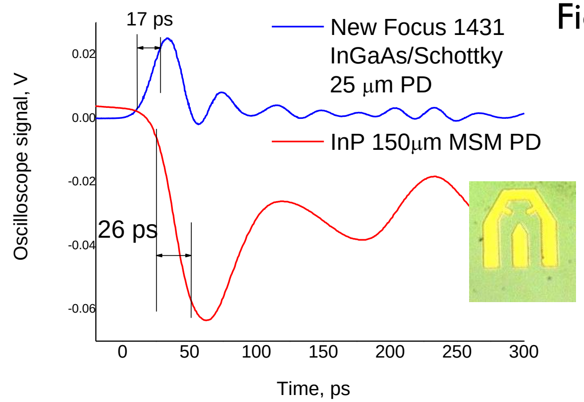


- Making a thin inversion layer increases UV efficiency but also increases sheet resistance
- Sheet resistance is high ~10 kΩ/sq.
- Fine in slow devices, but series resistance kills leading front

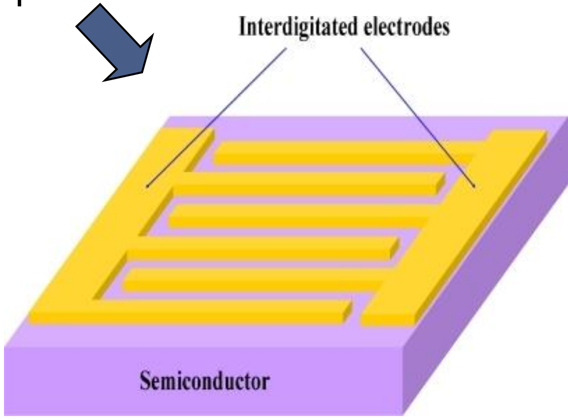
Geometry: Lateral vs. Vertical



Vertical:
Top and bottom contacts
Field normal to the surface

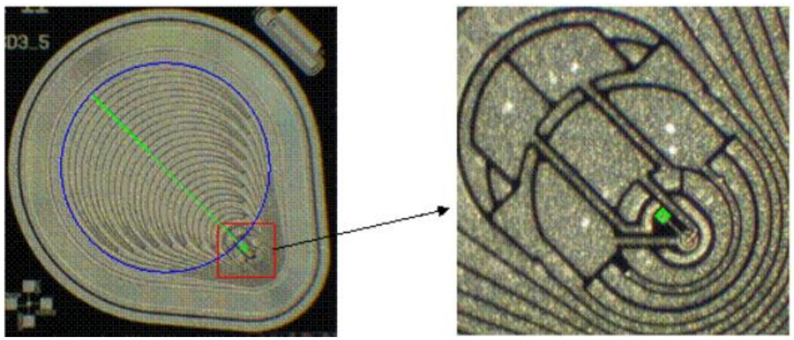


Lateral:
Both contacts on one surface
Field parallel to the surface



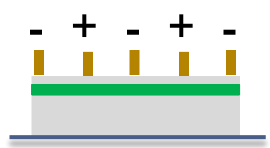
Vertical (p-i-n)	Lateral (MSM)
Large area contact, usually thin depletion layer, higher C	Small area contact, large gaps between electrodes, lower C
Surface dead layer due to top contact, bad for UV	No dead layer, large exposed surface, surface recombination
3D device, requires special packaging	Planar device, compatible with FET process, simple integration
Most common semiconductor detector type	Some designs commercially available, e.g. MSM's or Si drift detectors

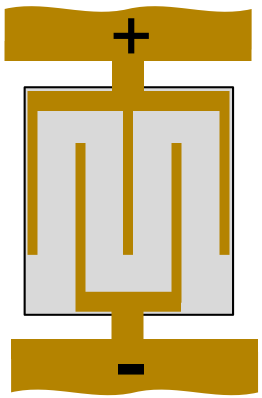
Silicon Drift Detector with integrated transistor [from PulseTor.com]

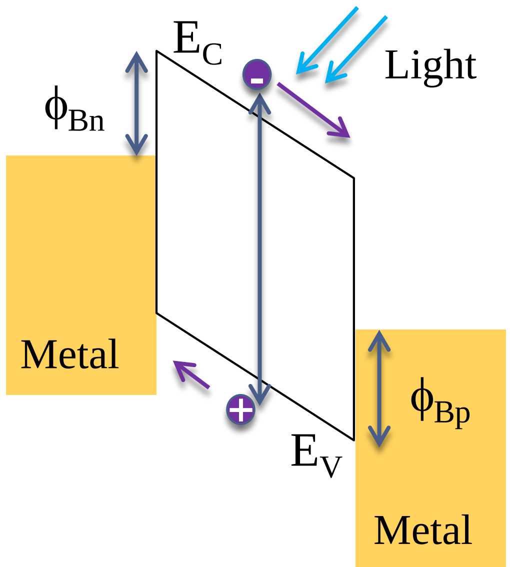


Metal-Semiconductor-Metal (MSM) PD

- The simplest lateral field detector is MSM structure which is back-to-back connected Schottky diodes







Advantages

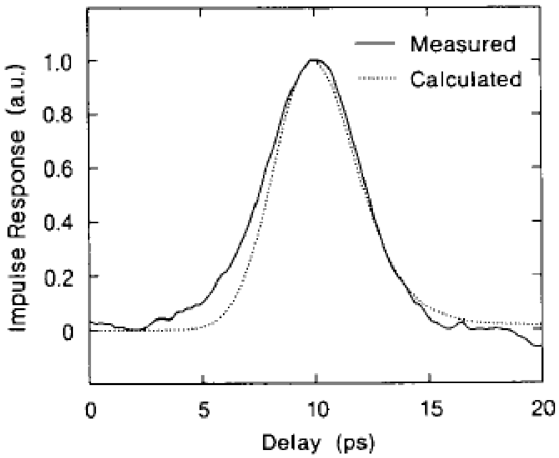
- Low capacitance per unit area
- Lack of dead contact layer (important to absorption coefficients $\alpha > 10^6$ cm^{-1} → 10nm absorption length)
- Reduced volume for generation-related dark current (in particular QW structures)
- Planarity, compatibility with FET process flow

Disadvantages

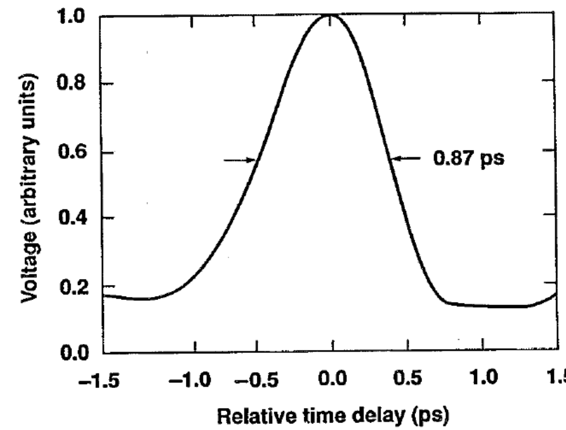
- Reflection from surface metal contacts
- Surface states enhance generation/recombination, reduce efficiency and increase dark current
- Metal-semiconductor interface is the origin of traps and leakage

Metal-Semiconductor-Metal (MSM) PDs

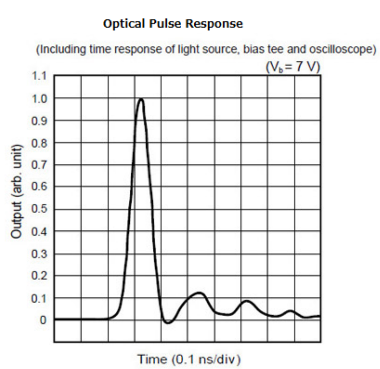
Zeghbroeck et al. , EDL 1988
GaAs MSM: 105 GHz, 5 ps (drift limited)



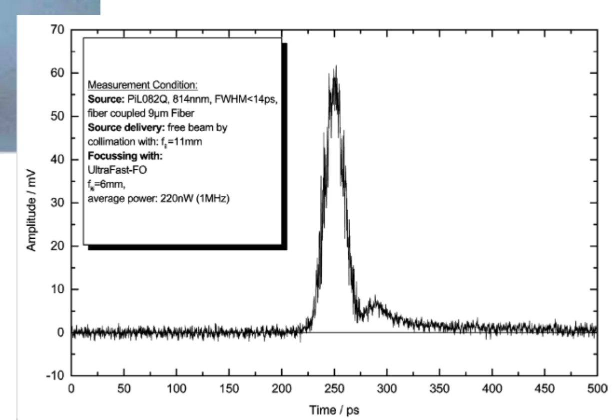
Chou et al. , APL 1992
LT-GaAs MSM: 0.87ps



Hamamatsu GaAs MSM
30 ps FWHM



Advanced Laser Diode Systems
InGaAs MSM: 20ps FWHMz



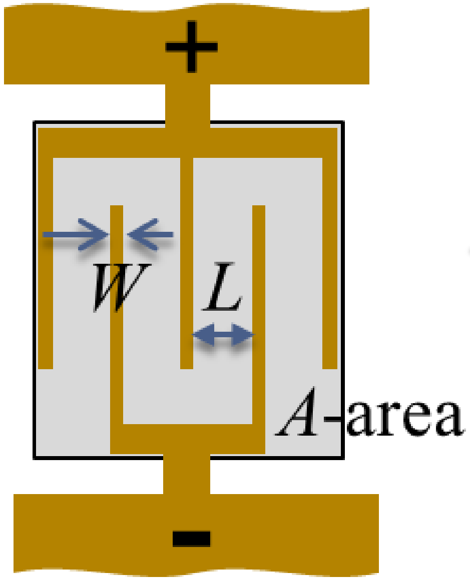
MSM PD: Capacitance

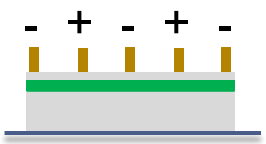
Capacitance of MSM device:

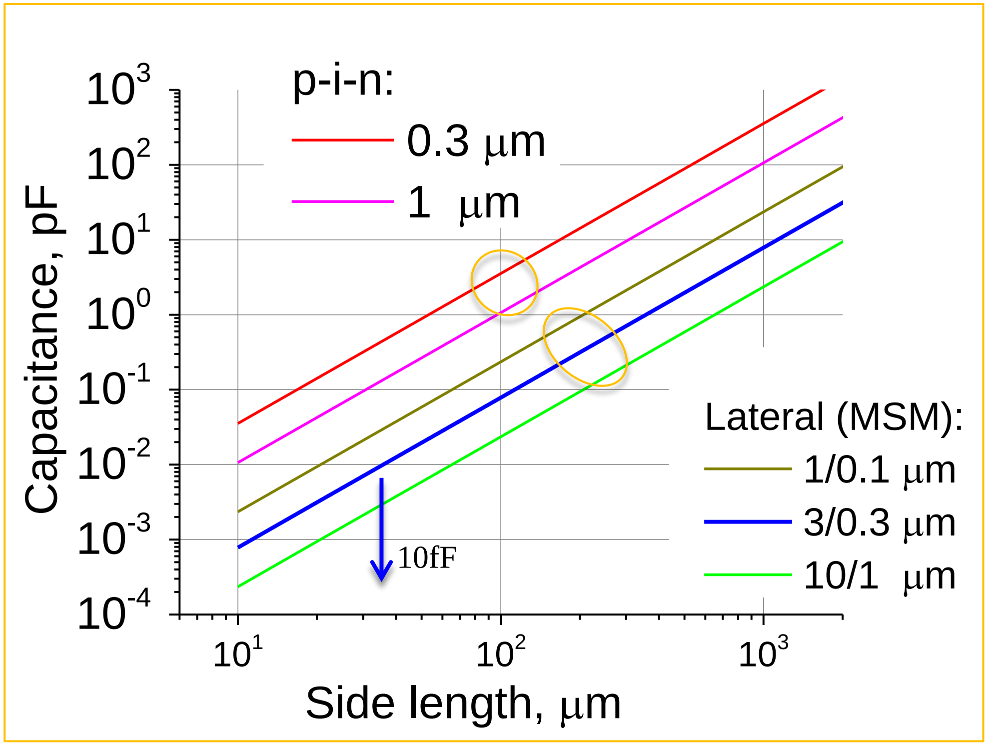
$$C = \frac{K(k)}{K\left(\sqrt{1-k^2}\right)} \frac{\varepsilon_0(\varepsilon+1)A}{4(L+W)}$$

$$K(k) = \int_0^{\pi/2} \frac{d\varphi}{\sqrt{1-k^2\sin^2\varphi}}$$

$$k = \tan^2 \frac{\pi W}{4(L+W)}$$







- MSM shows ~5x reduction of device capacitance (vs. pin) for the same drift length
- Capacitance reduction for the same TOF*: 15x as compared to Si p-i-n.

*TOF- Electron time-of-flight or drift time

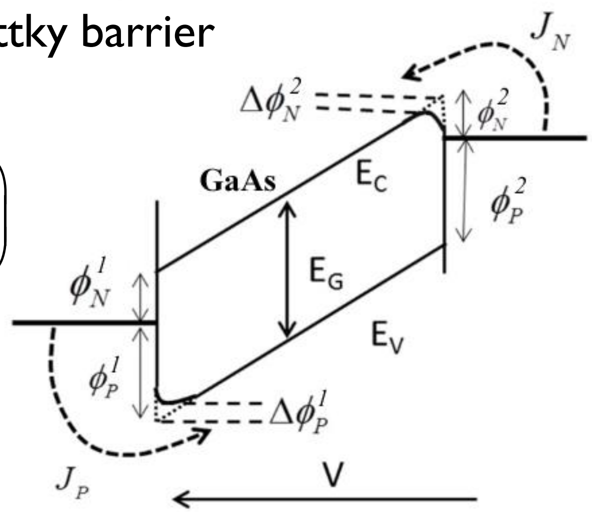
Dark current

- Shot noise is the major intrinsic noise source

$$\left\langle i^2_{PD\_noise} \right\rangle = \left(2qI_{tot} + \frac{4kT}{R_{eq}} \right) \Delta f \xrightarrow{\text{small signal}} 2qI_{dark} \Delta f$$

- Dark current in MSM is mostly due to thermionic emission over the Schottky barrier

$$J_{thermionic} \sim T^2 \exp\left(-\frac{q\phi_B}{kT} \right)$$



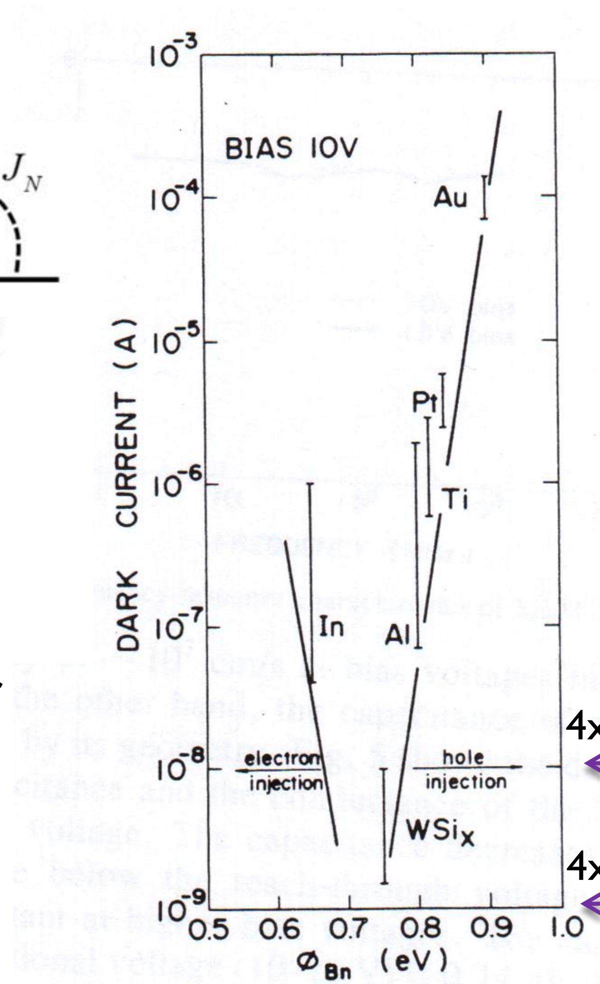
- Use of a contact on higher bandgap semiconductor (AlGaAs or AlInAs) lowers the dark current
- The lowest dark current in InAlAs/InGaAs heterostructure

  4.5×10^{-6} A/cm^2 [Kim et al. TED 51 351 (2004)]

- Compare to 5×10^{-11} A/cm^2 for Si p-i-n PDs

Dark curent in GaAs MSM

[Ito et al. JQE 22 1073 (1986)]

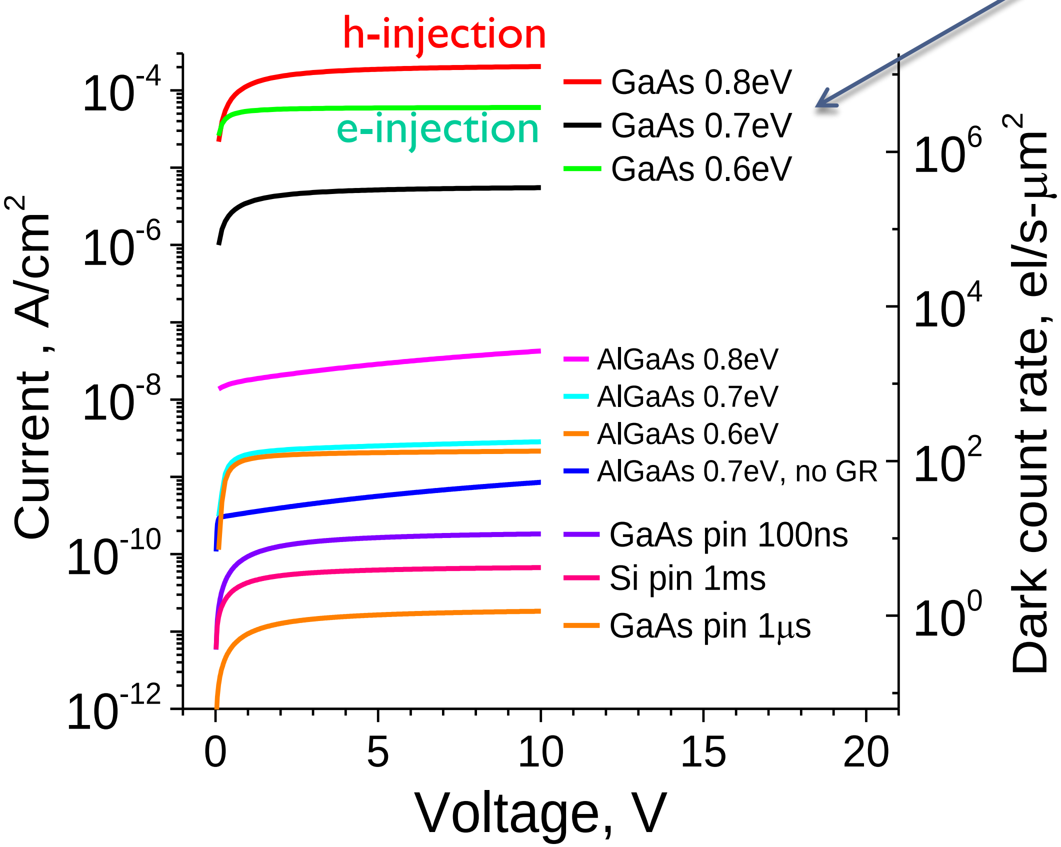


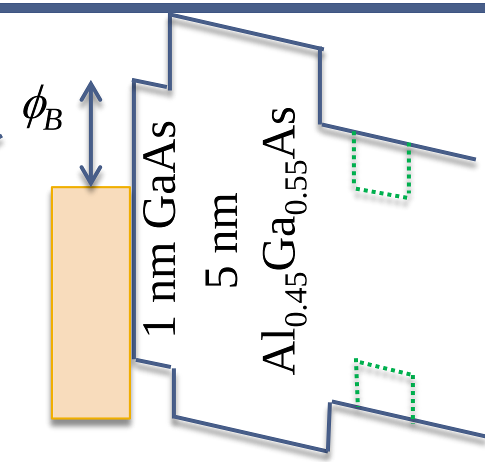
4×10^{-4} A/cm^2

4×10^{-5} A/cm^2

Dark current

Dark current in 1µm GaAs MSM and p-i-n diodes: effect of thermionic emission and generation





- A simple built-in heterojunction barrier close to Schottky contact can reduce current by 3-4 orders of magnitude to ~100 el/s-µm^2
- It can be further reduced by introducing p-n junctions instead of Schottky junctions
- Feasible to have one heterojunction and another Schottky junction
- Then dark current is limited by generation current:

$$I_{SHR} = qV_{depletion}\frac{n_i}{2\tau_o}$$

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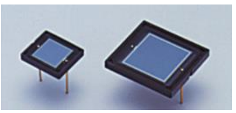
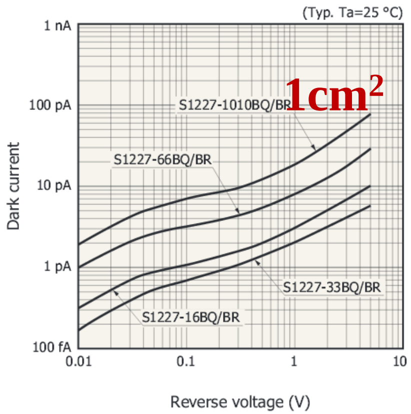
Dark currents in p-i-n PDs

Dark current in Si p-i-n PD

[hamamatsu.com]

S1227 series

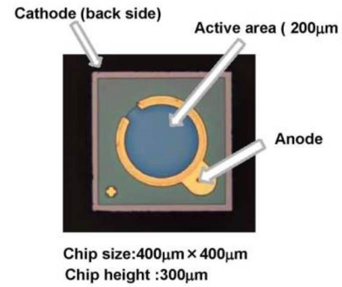




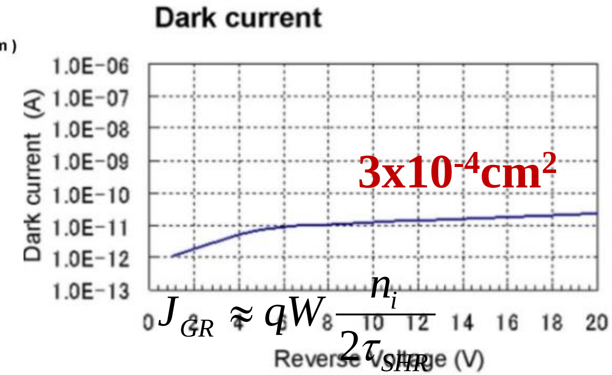
Dark current = 0.1nA/cm^2

Dark current in GaAs p-i-n PD

[kyosemi.co.jp]



30nA/cm^2



$$J_{GR} \approx qW \frac{n_i}{2\tau_{SHR}}$$

Generation dark current in W=0.5 µm pin diodes

Material	n_i, cm^{-3}	τ_{SHR}, s	J_{GR}, A/cm^2
Si	1.5x10^{10}	10^{-3}	6x10^{-11}
GaAs	1.8x10^{6}	10^{-8}	7x10^{-10}
$Al_{0.3}GaAs$	1.7x10^{3}	10^{-10}	7x10^{-11}

$$J_{GR} \approx qW \frac{n_i}{2\tau_{SHR}}$$

- Reverse current is ~2 orders of magnitude higher in GaAs than in Si p-i-n's
- There are number of reports of lower reverse currents, i.e. ~50 pA/cm^2 in p$^+$-p-n$^+$ [Chen et al. J. Phys.D, 44 215303 (2011)]
- Generation current is scaling as volume of the depletion region. Effective volume can be reduced in lateral structure

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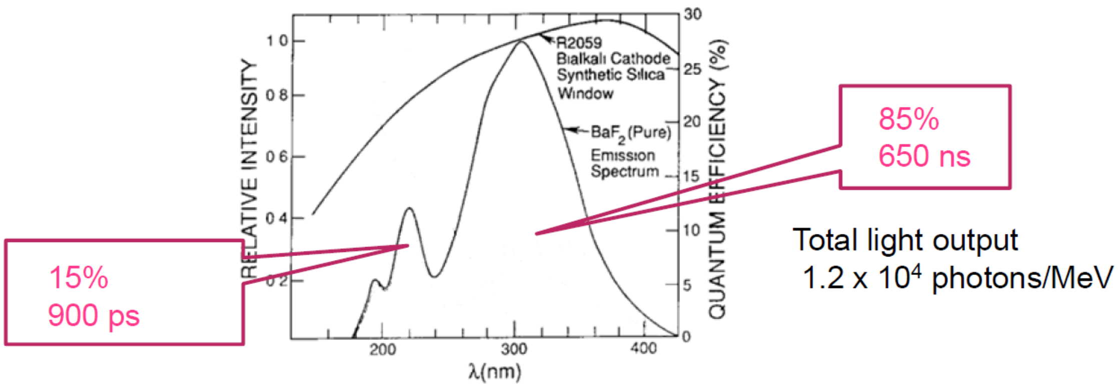
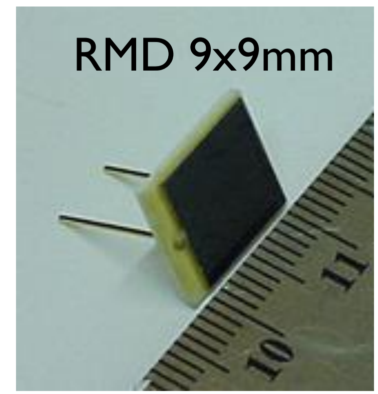
Si APDs: State-of-the-Art

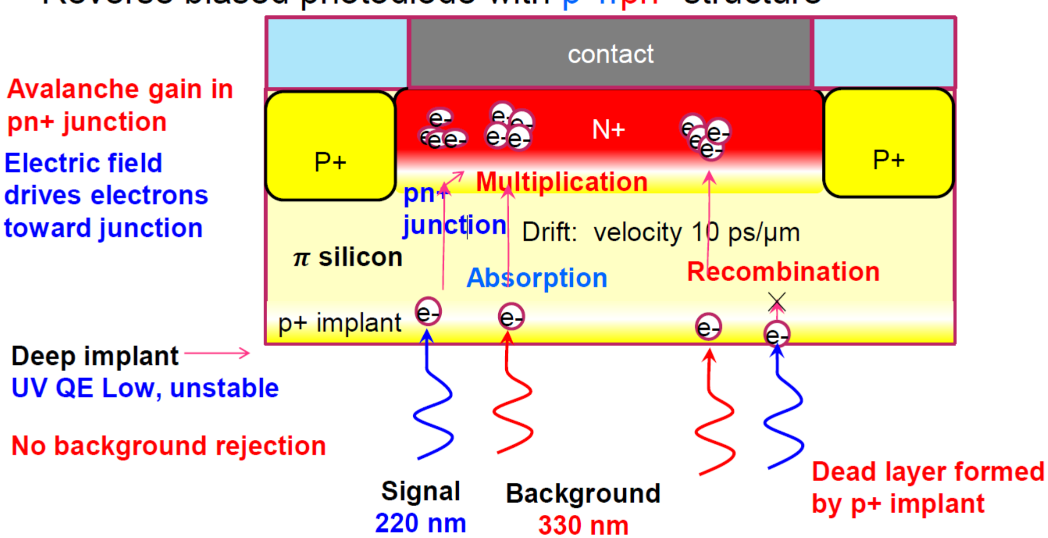
From D. Hitlin, CalTech/RMD/JPL, 2013

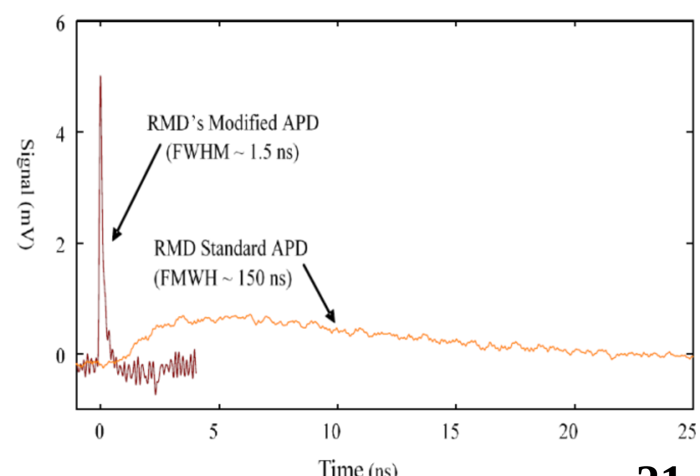




Reach-Through Avalanche Photodiode (RTAPD)

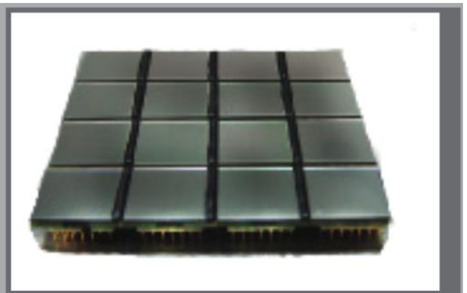
Reverse biased photodiode with p$^+$πpn$^+$ structure





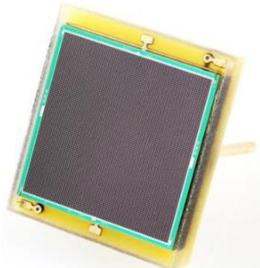
Next step: Sensor Partitioning

RMD SSPM: 130 fF/pixel (pixel size ~50µm)



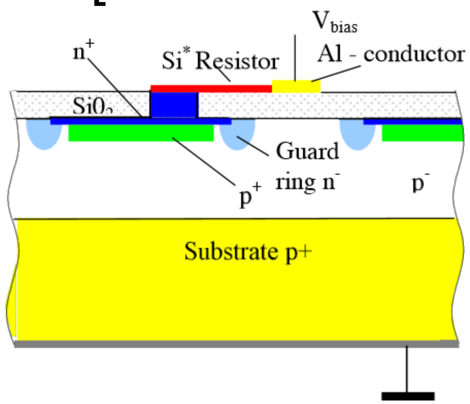
4 x 4 Array of 1cm x 1cm SS223-2 chips
(4 Arrays = 1 SSPM)

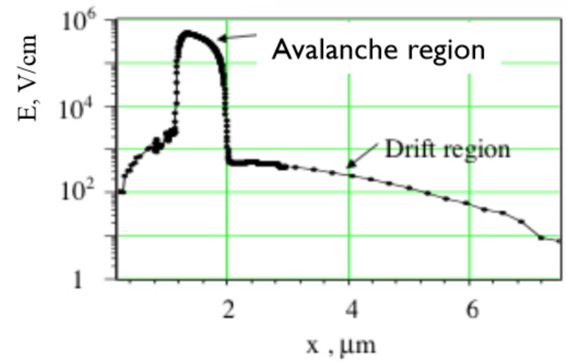
KETEC SSPM



SSPM: APD array in parallel

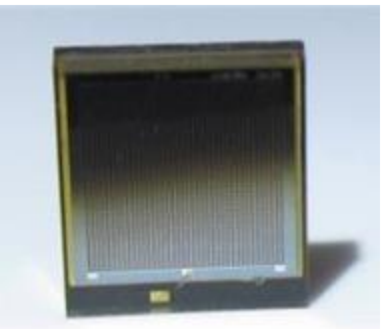
[From: "Scintillation Detectors", U. of Heidelberg]



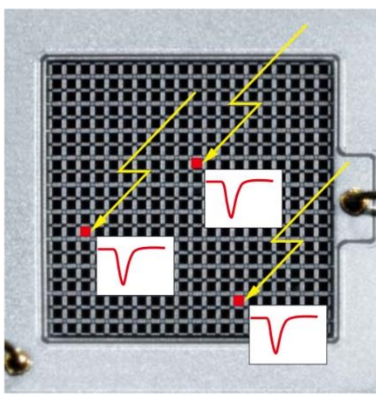


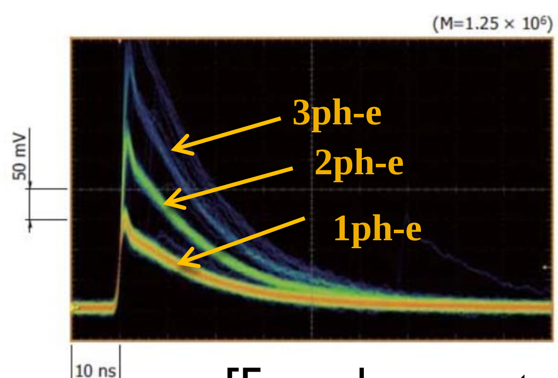
- Geiger-mode: Gain ~10^6
- ns-range device: best jitter ~100ps

AdvanSiD SSPM



Hamamatsu SSPM: S12571



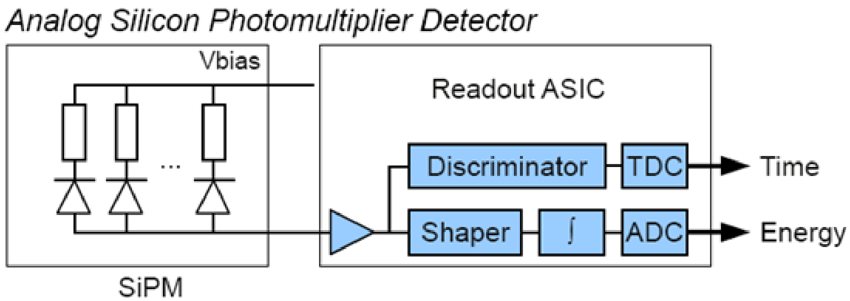


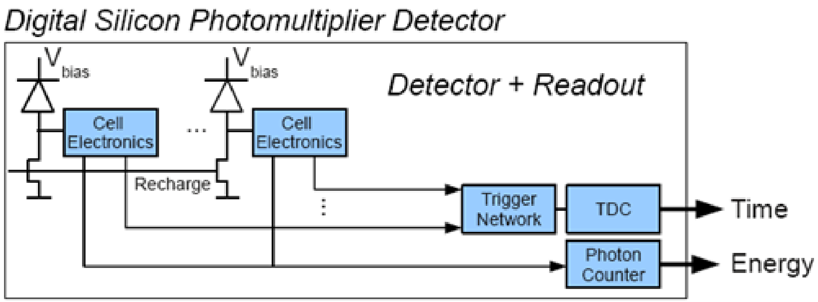
[From hamamatsu.com]

State of the art: Digital SiPM

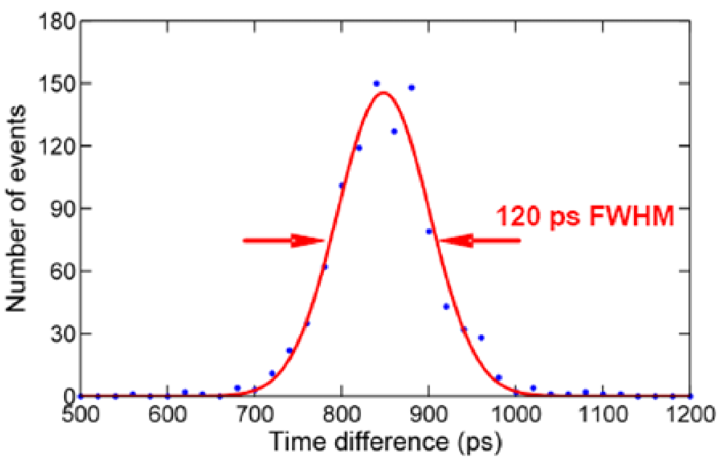
Philips Digital SSPM

[From: www.research.philips.com and PDPC presentation, 2012]

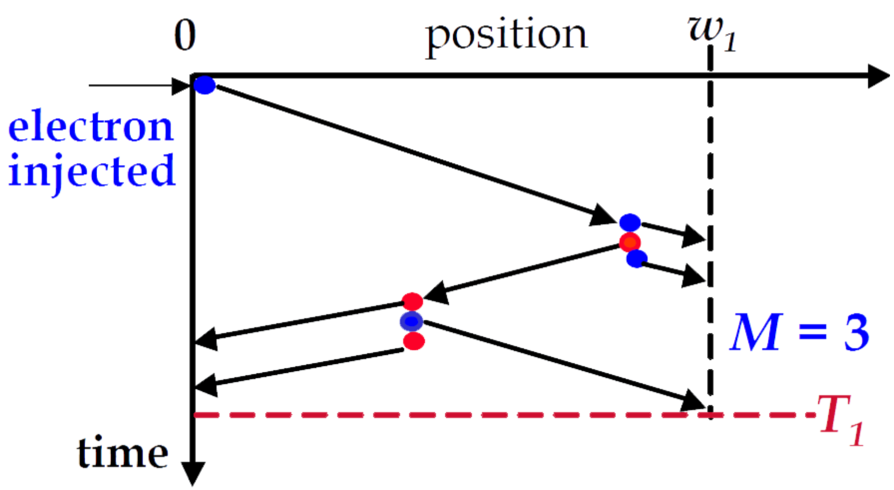




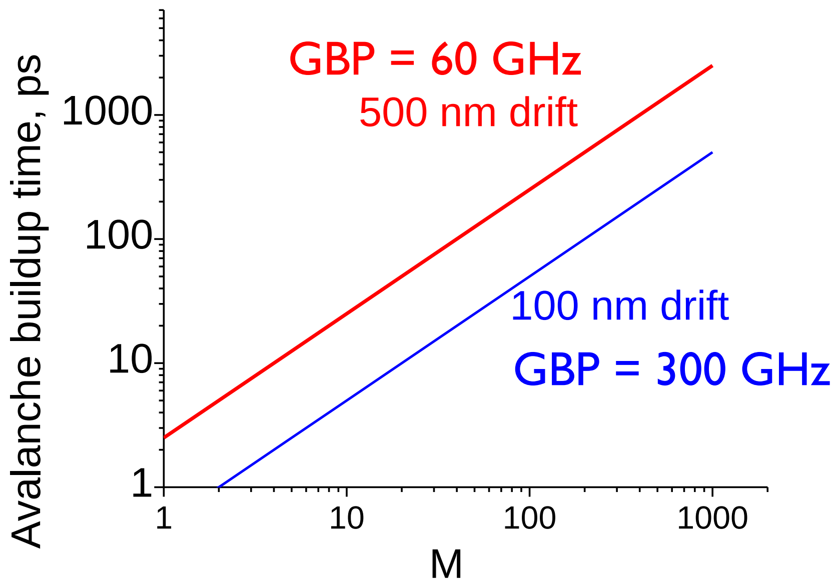
- Digital SiPM: each pixel contains its own electronics
- Low parasitic capacitance → reduced gain → improved stability



Fast APDs: Multiplication Buildup

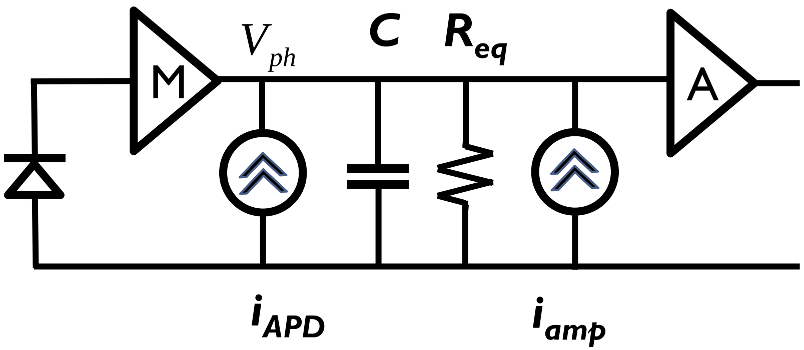


Avalanche buildup time for GaAs SAM APD



- Multiple transits in APDs reduce speed (multiplication buildup time)
- Geiger mode does not provide benefits
- Multiplication length can be reduced to >100nm to increase speed
- Demonstrated gain-bandwidth product ~300-400 GHz

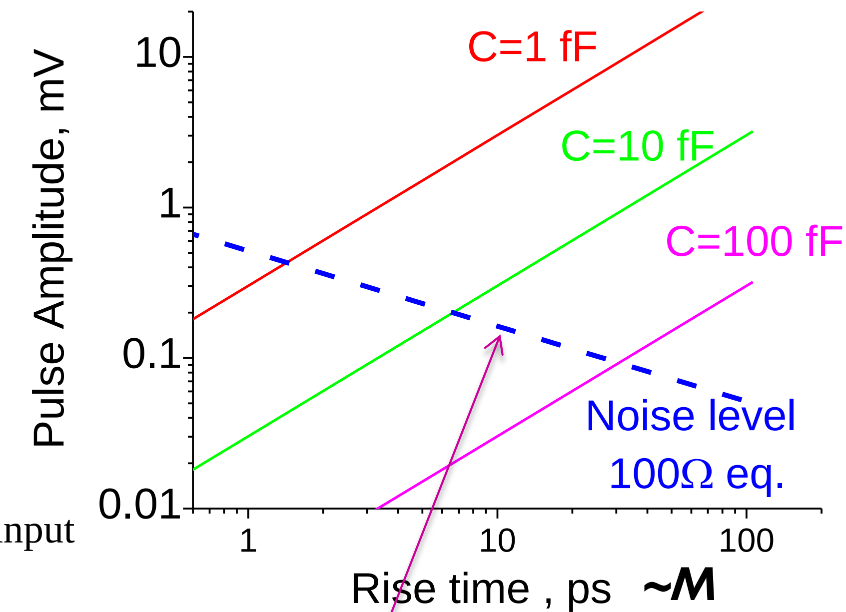
Fast APDs: S/N for single photoelectron detection



$$V_{ph} = \frac{I_{ph}\tau}{C} \xrightarrow{\text{single p.e.}} \frac{Me}{C} \qquad R_{eq}C << \tau$$

$$v_{noise}^2 = 4\pi kTR_{eq}\Delta f$$

For single photoelectron detection for GBP= 300 GHz



Dependent parameters:

- Fixed **rise time** τ limits **multiplication** M (fixed GBP)
- **Multiplication** M determines **total charge** at amplifier input
- **Signal voltage** determined by charging the **capacitor**
- **Noise** of an amplifier input determines **maximum capacitance**

- **Limited room for variations!**
  - Capacitances of ~10 fF are needed to obtain reasonable S/N ratio at low M's
  - Need for low-C integration of the PD with amplifier → monolithic integration

For S/N = 1:
M=20
C=20 fF

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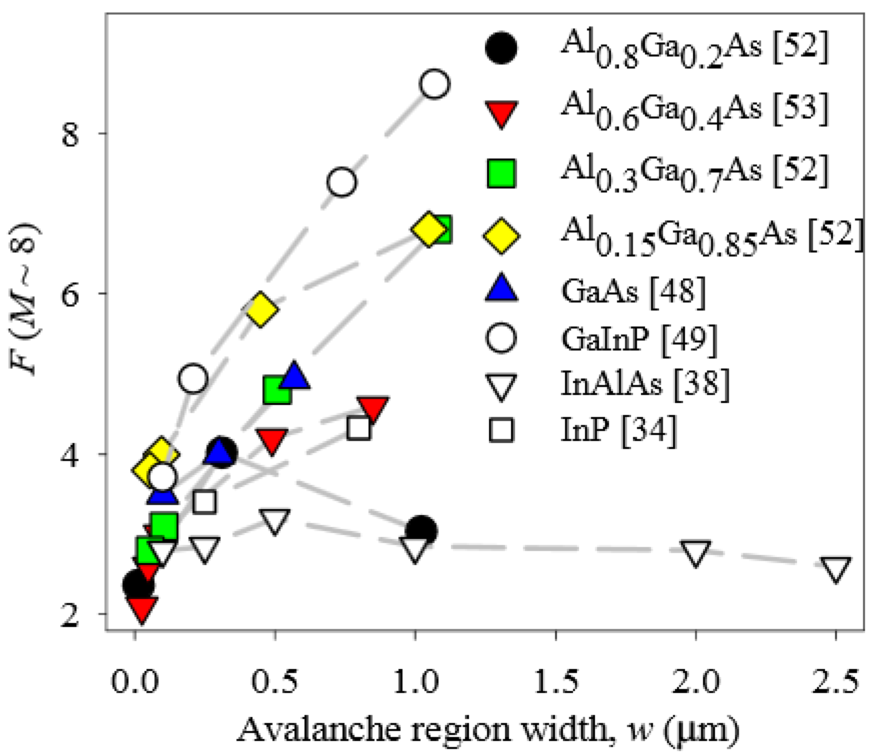
Improvement of APD noise: $Al_{0.8}Ga_{0.2}As/GaAs$

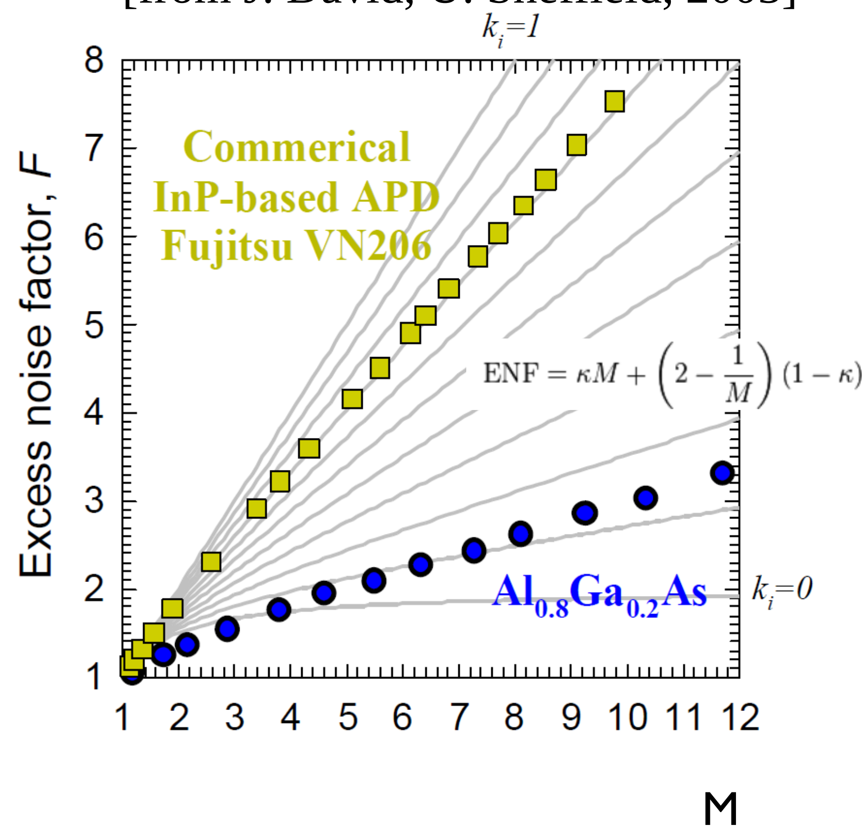
Exceess noise in III-V APDs

[Xi, PhD thesis U. Sheffield, 2012]



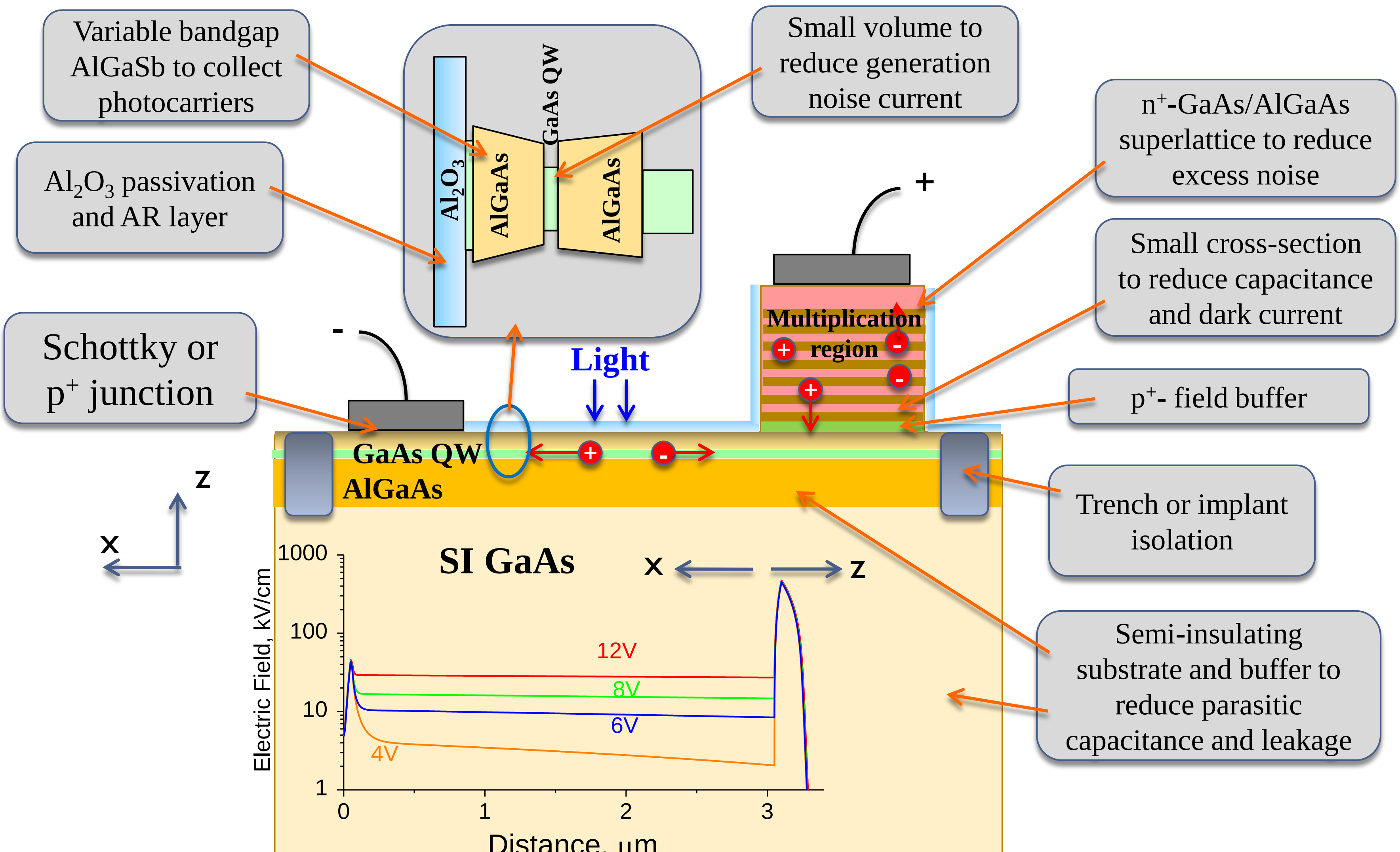
Comparison of $Al_{0.8}Ga_{0.2}As$ and comercial InP APDs

[from J. David, U. Sheffield, 2003]



- Commercial InP-based APD give excess noise of k_i=~0.7
- Much lower excess noise can be obtained with wider bandgap III-V's, e.g. $Al_{0.8}Ga_{0.2}As$ as avalanche medium

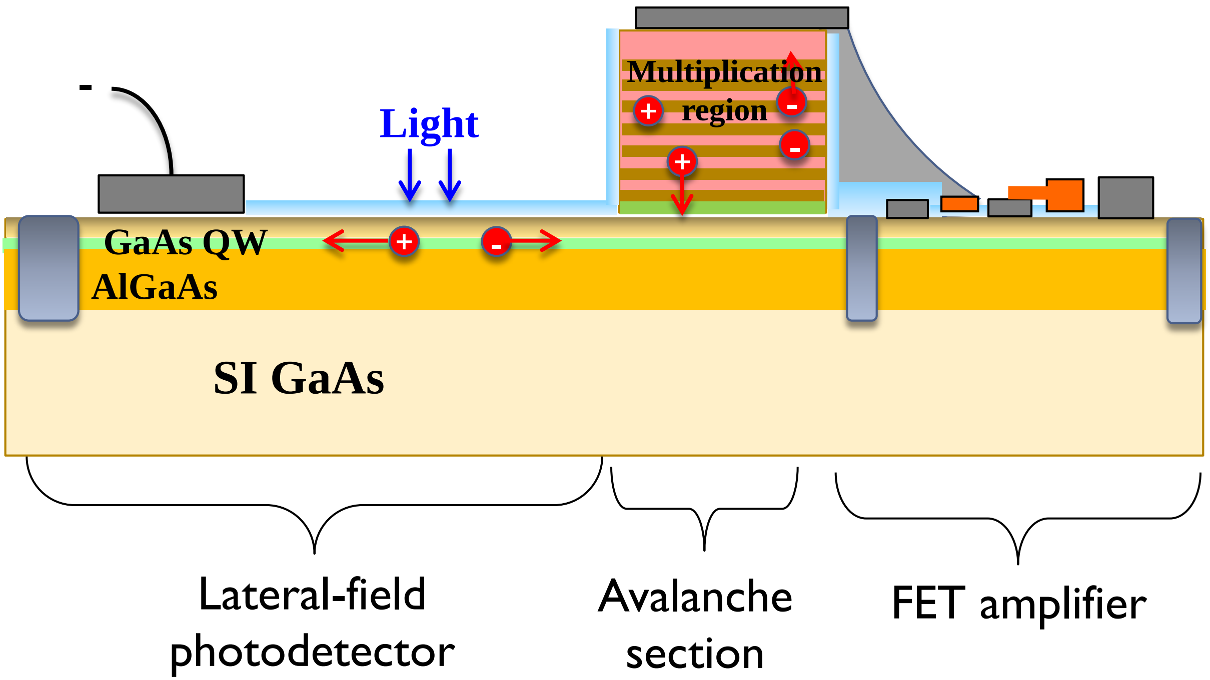
Concept for ps APD



PD Integration

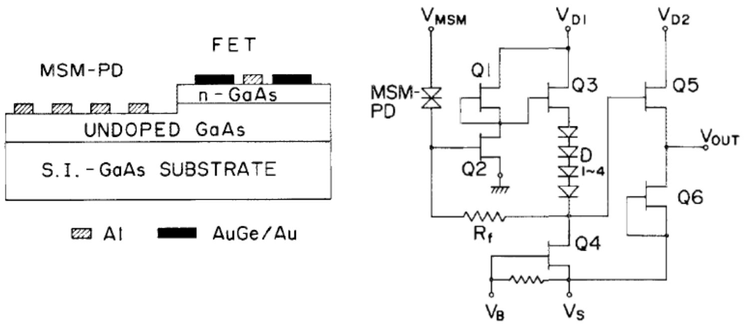
Integration with a transistor amplifier:

- FET uses same basic technology
- Possibly uses same QW as a photodetector
- Area separated by insulating trench or implant within the same pixel
- Integration of planar detector with FET previously demonstrated



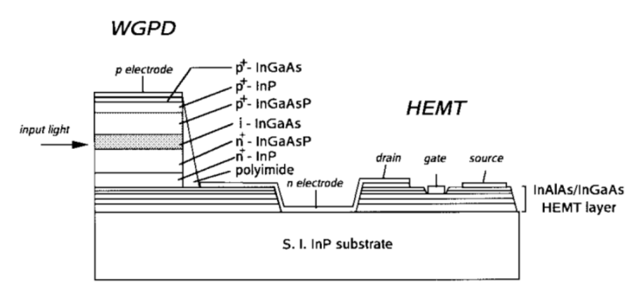
Integration of GaAs MSM with MESFET

[Ito et al. APL 47 1129 (1985)]

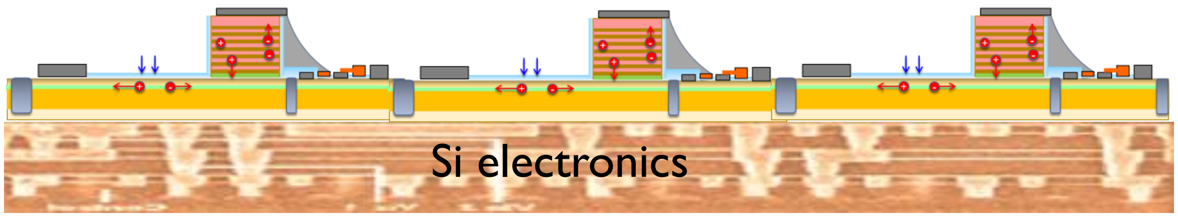


Integration of InGaAs MSM with HEMT

[Kato,TMTT 47 1265 (1999)]



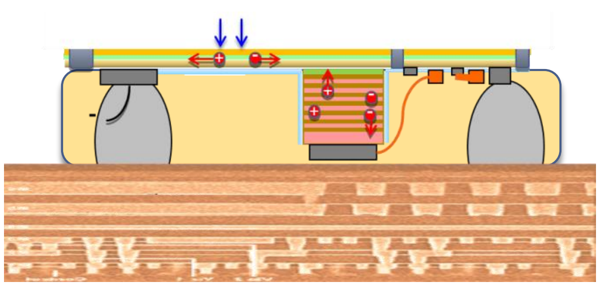
PD Integration: Si platform



Finally: Partitioning and Integration with electronics (Si)

Face-up mounting of thinned GaAs wafer to Si

- Larger openings to run conductors to Si
- Still front side illumination
- Lost system area for electrical connections



Face down (flip-chip)

- Established technology using solder bumps, e.g. for FPAs
- Backfill with polymer for mechanical stability
- Minimizes interconnect problem
- Requires precise substrate removal: oxidation lift-off

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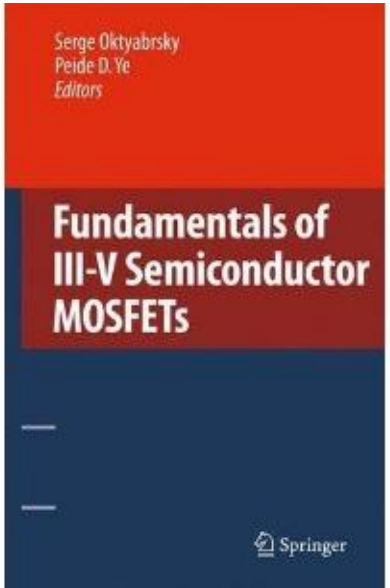
III-V Materials in Mainstream (Si) Electronics

III-V MOSFETs (and FinFETs) is extremely hot and fast developing topic pursued by many IC manufactures: INTEL, GlobalFoundries, IBM, TSMC, Samsung…

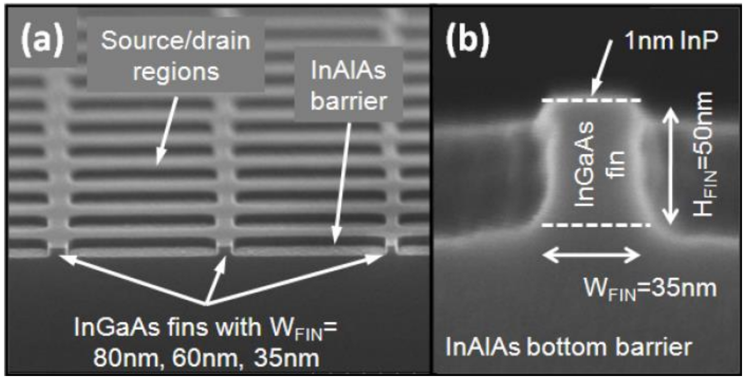
Tool manufactures (AMAT, TEL,…) and pilot IC R&D's (Sematech, IMEC) are adapting existing Si technologies / toolsets for III-V's

Silicon Semiconductor, 2013

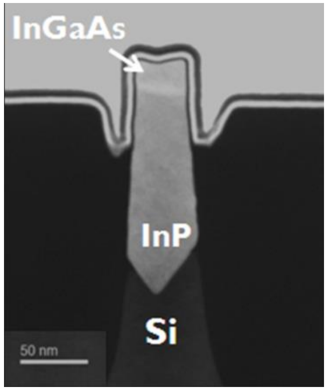
2010



INTEL InGaAs FinFET (2010)



IMEC's InGaAs FinFET (2013)

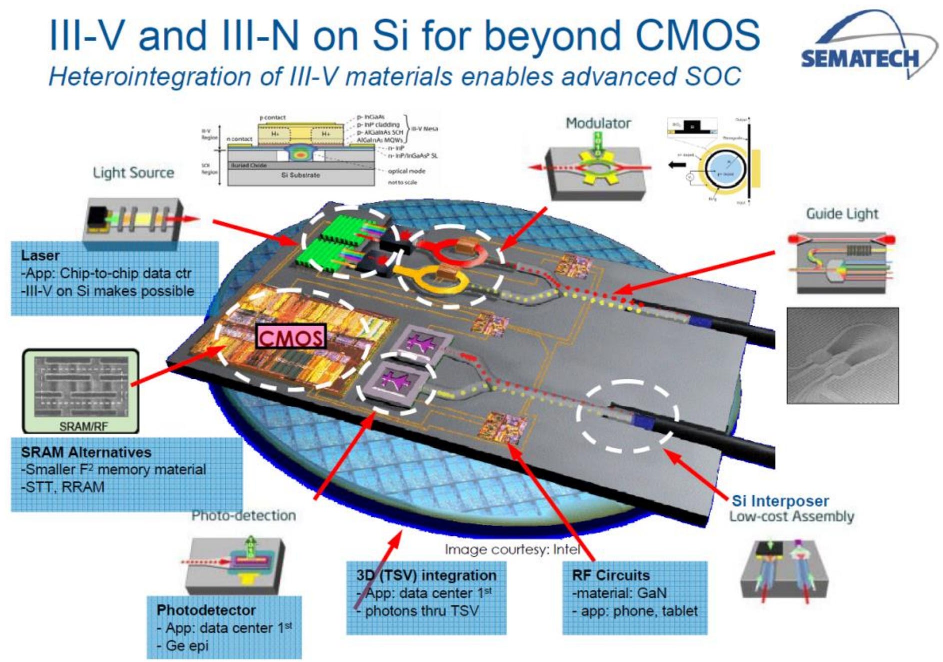


Si Industry - First III-V MOCVD Laboratory

Aixtron 300mm MOCVD tool for III-V on silicon processes

300 mm Si wafer and shower-head

Integration on Si: from R. Hill, Sematech 2013



Aixtron G5 HT MOCVD* system operated by SEMATECH and CNSE:

- III-As and III-N growths
- MO and hydride precursors
- In-situ cleaning

* MOCVD – metal-organic chemical vapor deposition

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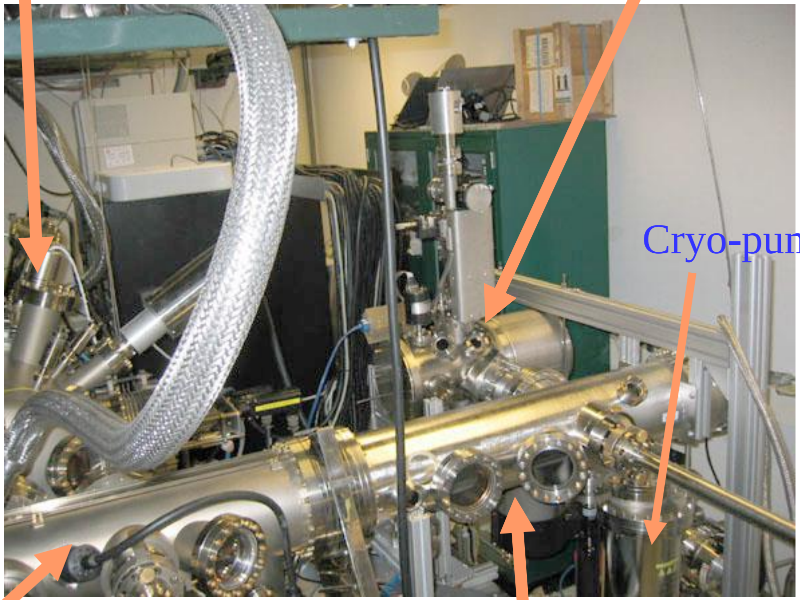
Molecular Beam Epitaxy (MBE) Laboratory



- MBE Veeco Gen II system:
  - Duo-chamber MBE system for As- and Sb- based III-V's
  - Triple-magnetron sputtering chamber (HfO_2, TaN, TiW)
  - Reactive e-beam evaporator (HfO_2 and Al_2O_3)

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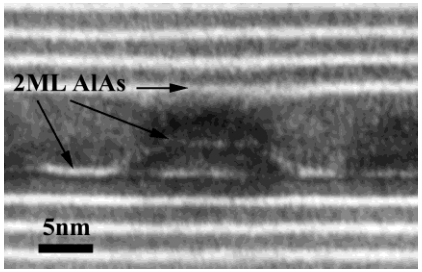
Compound Semiconductor Materials and Devices: Examples

Shape-engineered QD

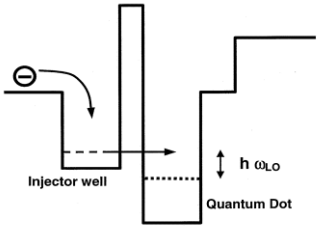


Materials/Technologies

- MBE III-As and III-Sb
- Entire in-house processing
- Heterostructures
- In-situ (UHV):
  - High-k oxides
  - Contacts and Metallization

Quantum dots – related application

- Tunnel-coupled QD-QW VCSEL
- QD SLED for OCT
- Media with controlled photo-electron kinetics

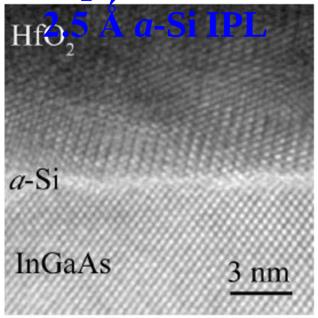


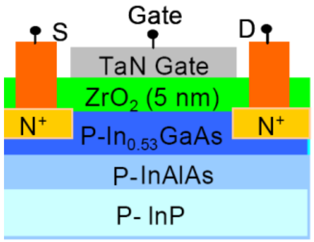
Electronic devices

III-V high-k MOSFETs

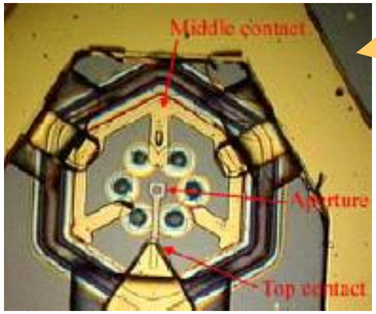
- In-situ high-k oxide for n-MOSFET
- High-mobility p-MOSFET
- Regrown source/drain

HfO_2/InGaAs with 2.5 Å *a*-Si IPL





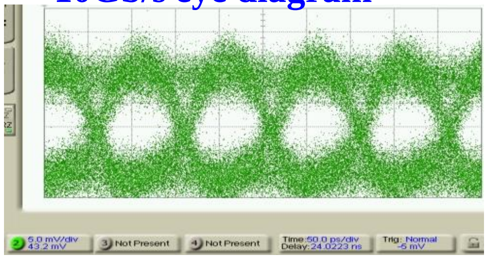
VCSEL-Modulator

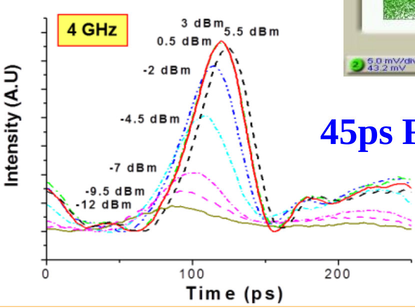


Photonic devices

- Cavity optical decoupling approach: duo-cavity VCSEL-modulator
- Q-switching with intracavity modulator
- Bragg MQW lattice
- QWIPs/QDIPs
- QD solar cells

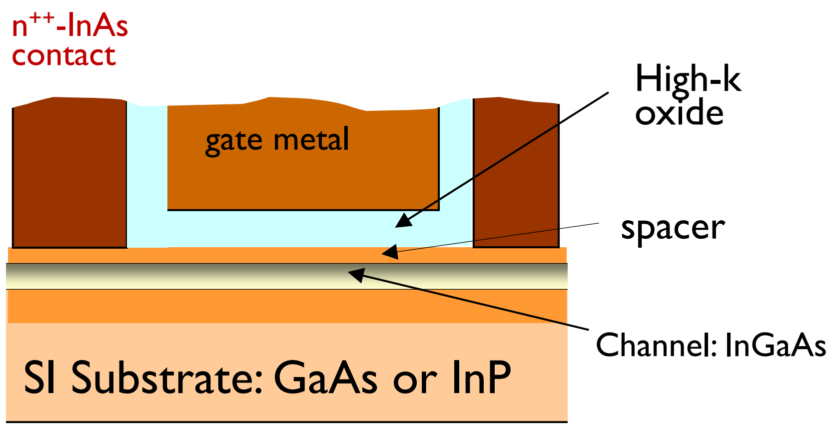
10Gb/s eye diagram

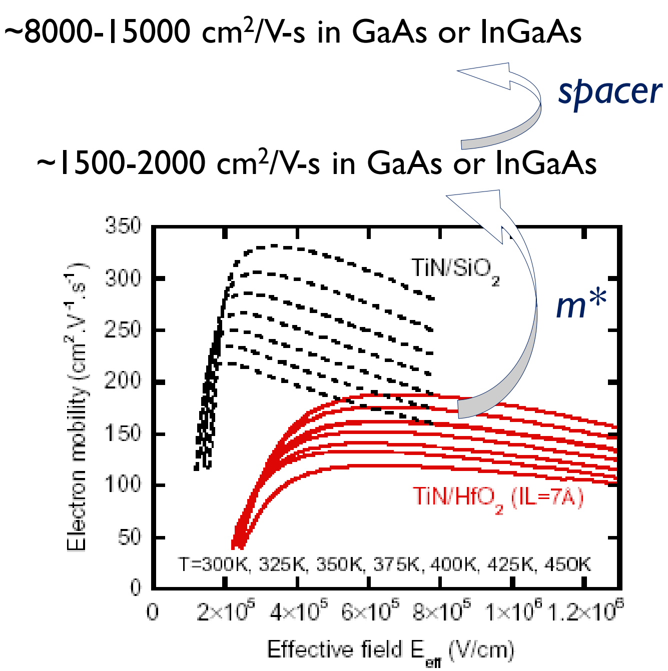




45ps FWHM Q-switch pulse generation

III-V/Oxide Interfaces: Challenges





From Weber et al. SSE 2006

- **High quality interface with dielectric (as SiO_2/Si):**
  - **Low surface recombination rate**
  - **Low density of interface states**
  - **High thermal and chemical stability of the interface**
- **Improvement of channel transport:**
  - **Low mass: Scattering – Coulomb, roughness, remote soft phonons**
  - **Buried channel**
- **S-D resistance**
  - **Regrown InAs for n-type or InSb on p-type**
  - **Epi-SD and gate-last flow**

GaAs/high-k Interfaces: Surface recombination

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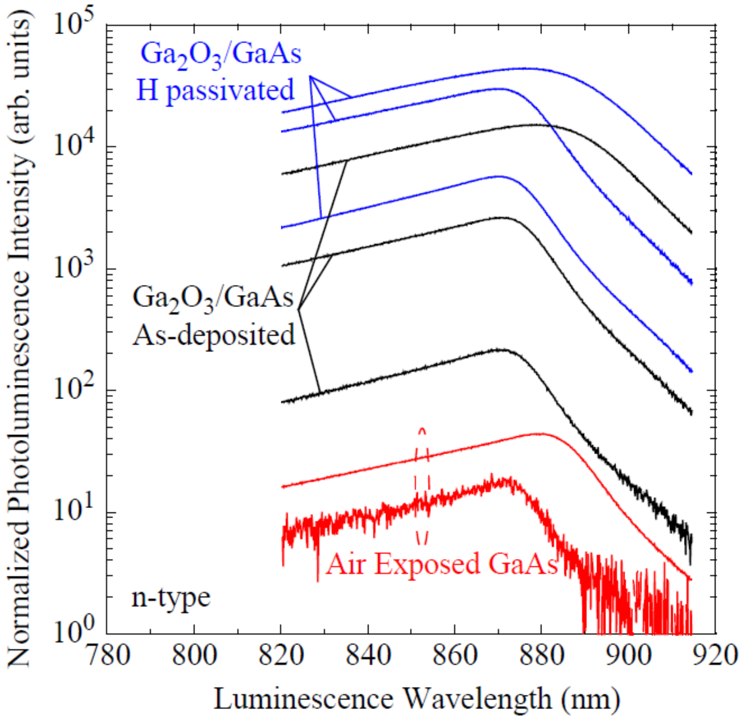
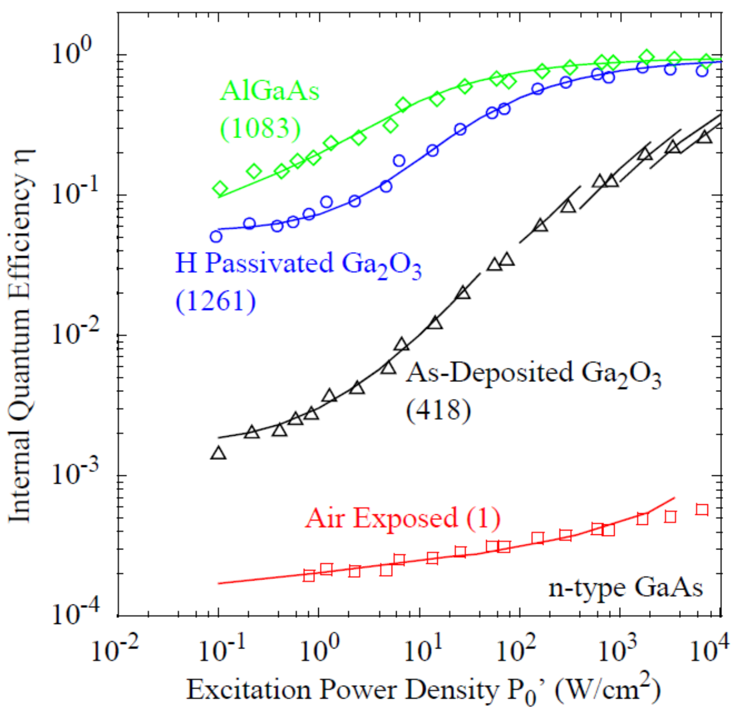
RT Photoluminescence and Internal Efficiency of GaAs with Different Surfaces

[Passlack, in "Materials Fundamentals of Gate Dielectrics…" 2005]





- Air exposed surface has high recombination velocity → kills photocarriers
- Great (~4-5 orders) reduction of the surface recombination demonstrated with various passivation techniques

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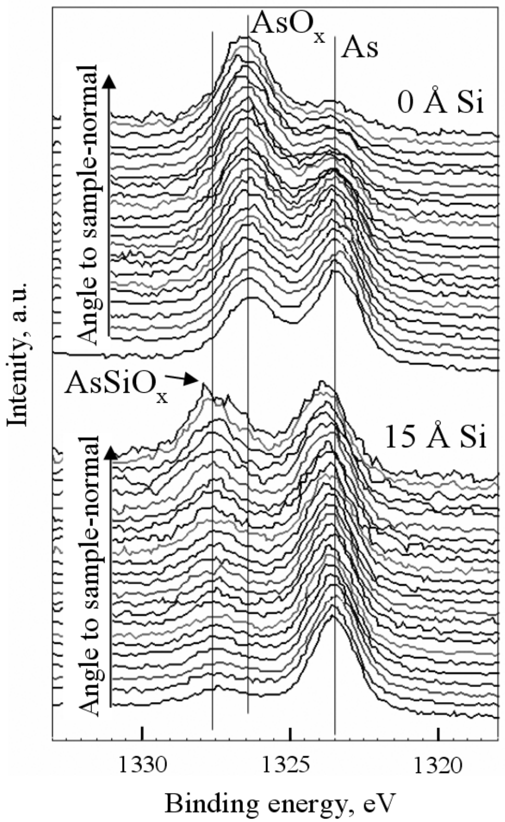
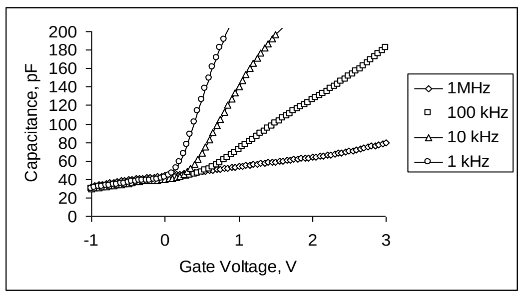
a-Si Interface Passivation of High-k/GaAs interface

1.5 nm a-Si on GaAs + PVD HfO_2

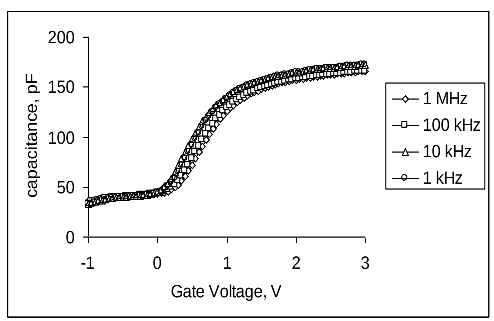
Angle-resolved As 2p XPS spectra and CV's



Fermi level is pinned

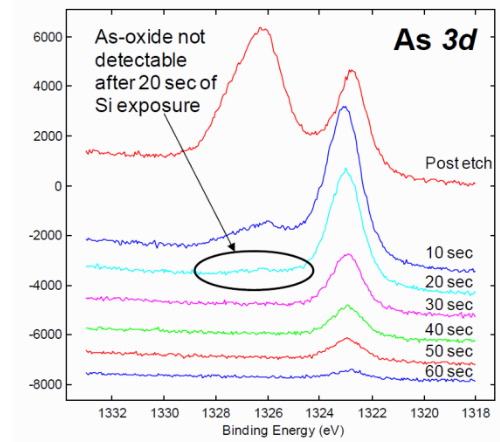


Fermi level is not pinned

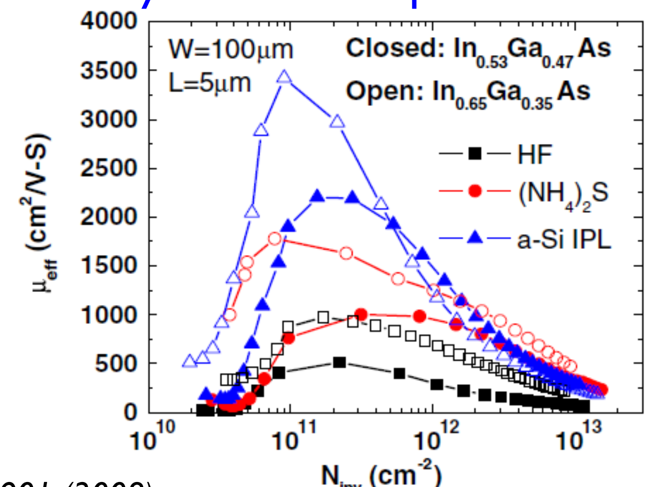


Wallace and Vogel groups, UTD

Removal of As-O with a-Si deposition



Eff. mobility vs. different passivation

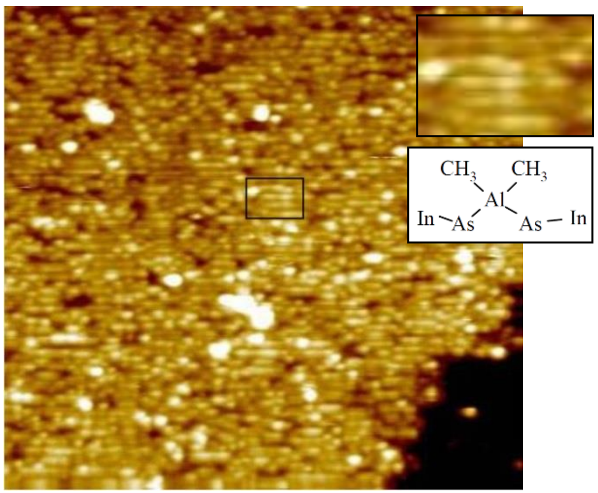


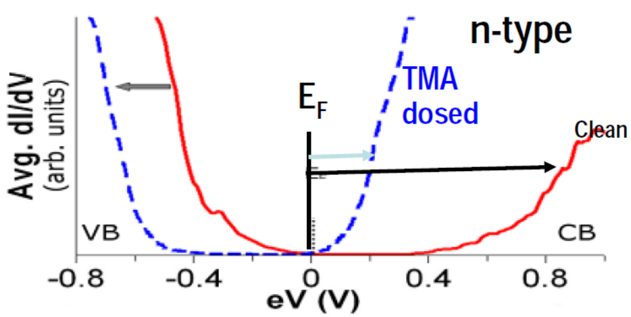
Koveshnikov, APL 88, 022106 (2006)
Oktyabrsky, Mat. Sci. Eng. B, 135 272 (2006)

Hinkle, APL 92, 071901 (2008)
Milojevic, APL 93, 202902 ; 252905 (2008)
Sonnet. Microel. Eng. 88, 1083 (2011)

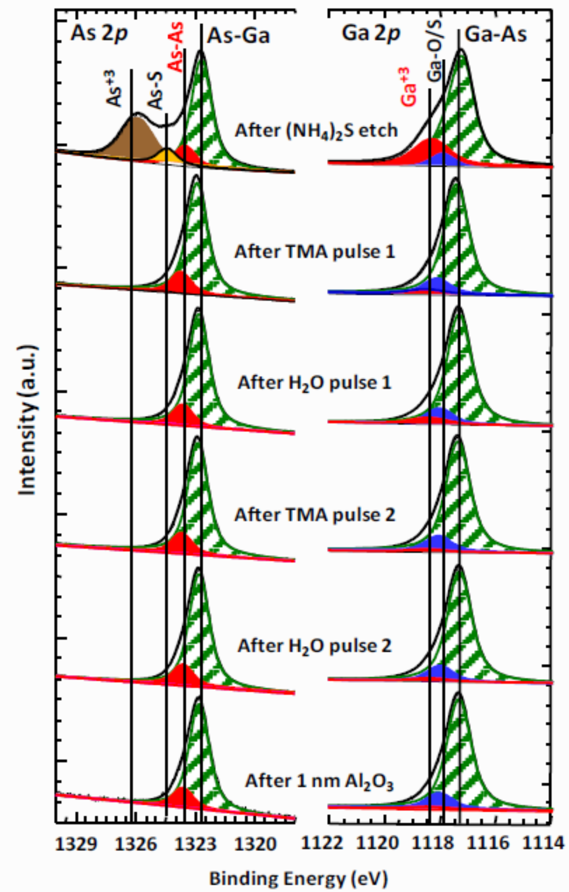
ALD Al_2O_3 : "TMA Self-Cleaning"

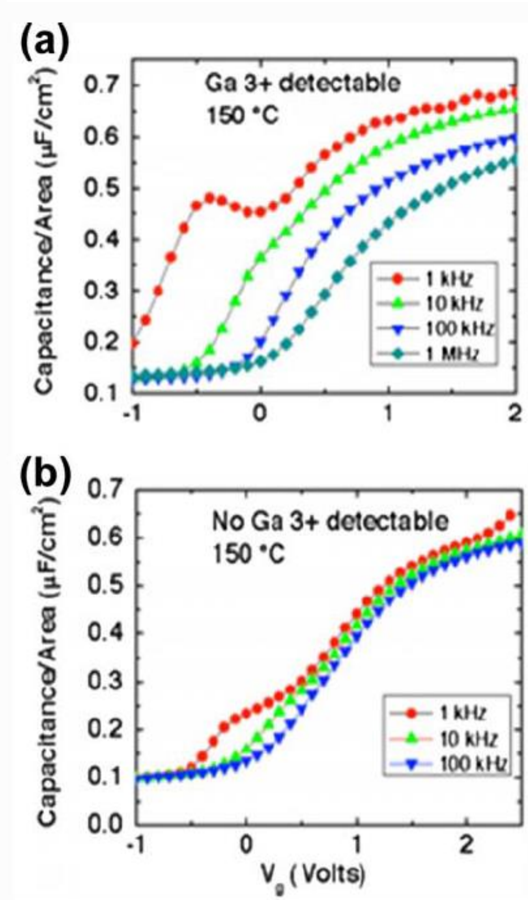
UHV STM and STS of TMA-exposed InGaAs surface (Kummel group, UCSD)





In-situ XPS and C-V (Wallace and Vogel groups, UTD)





- Saturation dose of TMA results in a near monolayer coverage with no substrate atom displacement
- TMA dosing restores the Fermi level to the CB edge

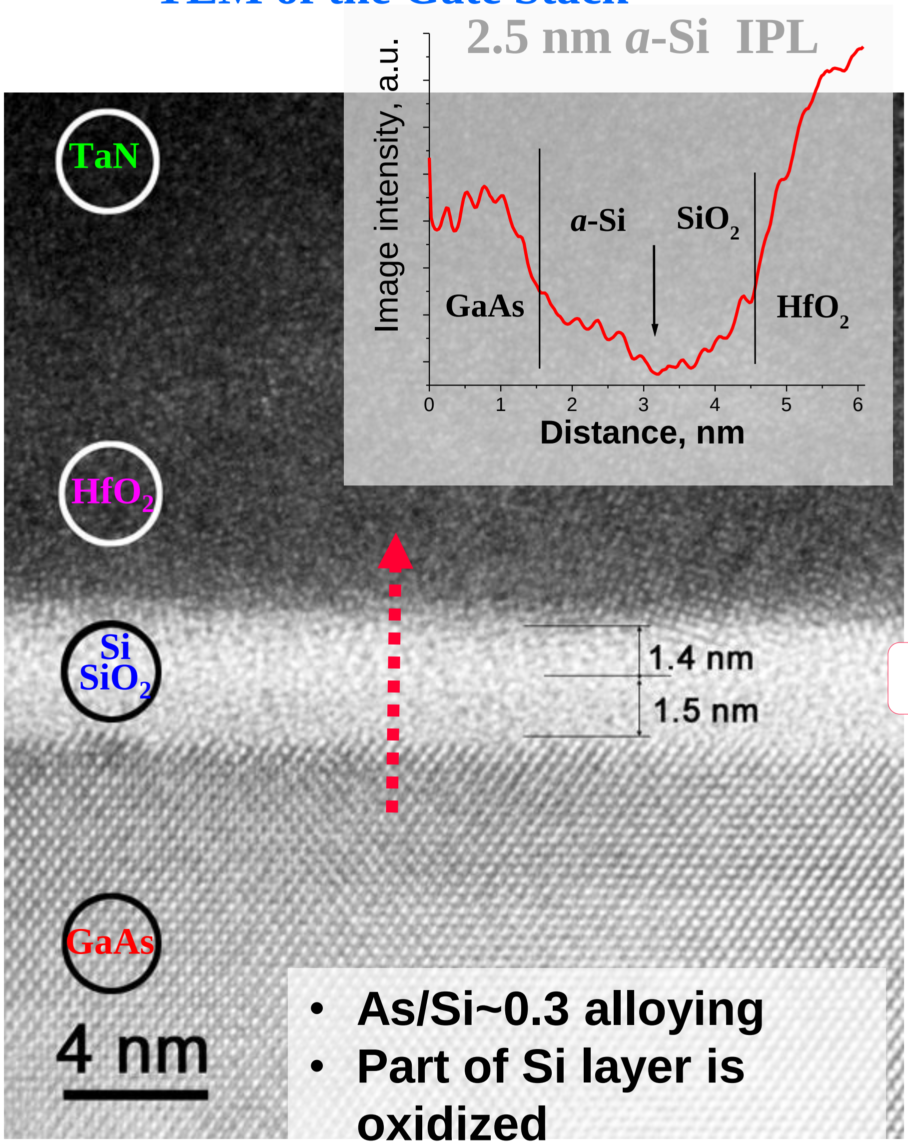
Kummel ISAGST (2011)

- TMA is efficient to remove Ga- and As-oxides
- As-As dimers is the major component left

Wang Microel. Eng. 88, 1061 (2011)

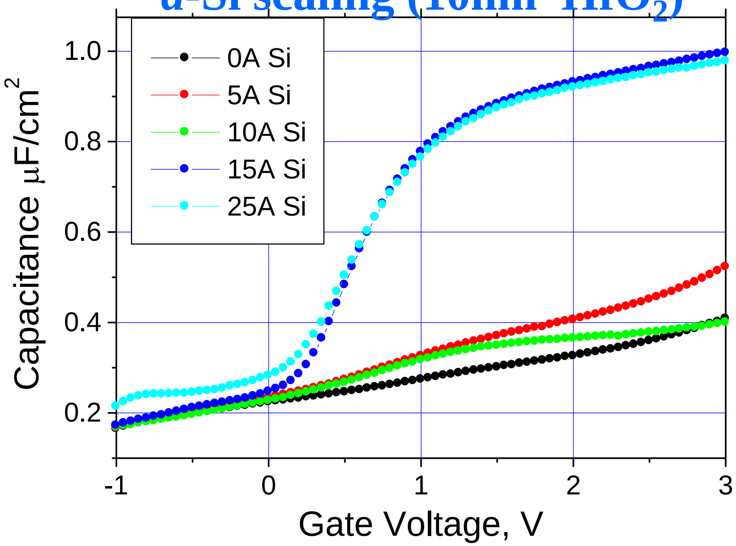
HfO_2/a-Si/GaAs High-k Gate Stack

TEM of the Gate Stack

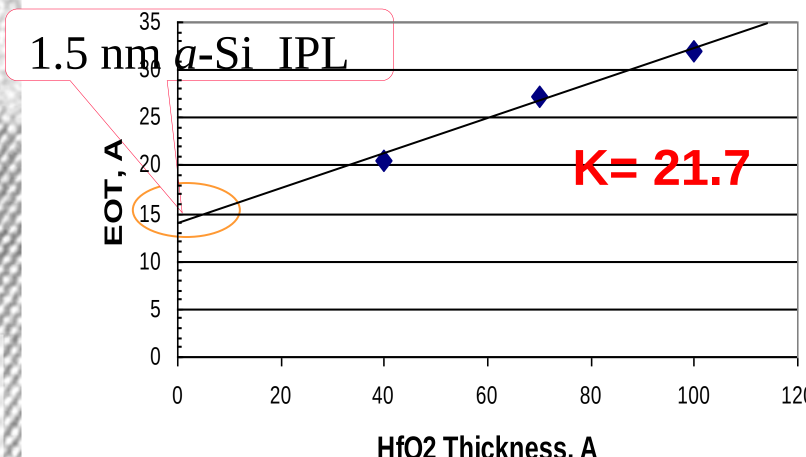


- As/Si~0.3 alloying
- Part of Si layer is oxidized

a-Si scaling (10nm HfO_2)



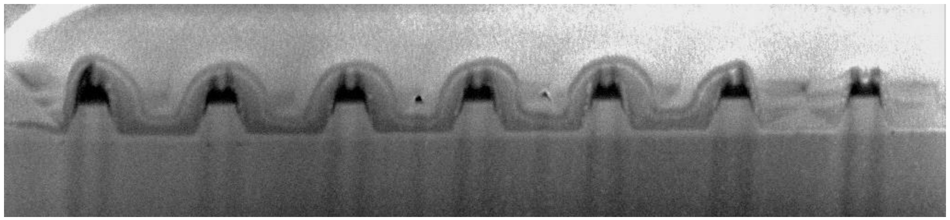
HfO_2scaling (1.5 nm *a*-Si)



- The k-value of the HfO_2 gate oxide ~21-22

III-V Processing

E-beam lithography process for FinFET fabrication

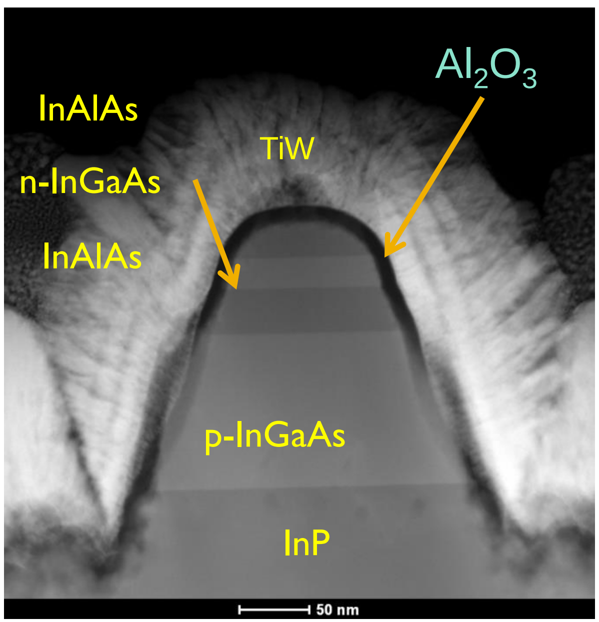


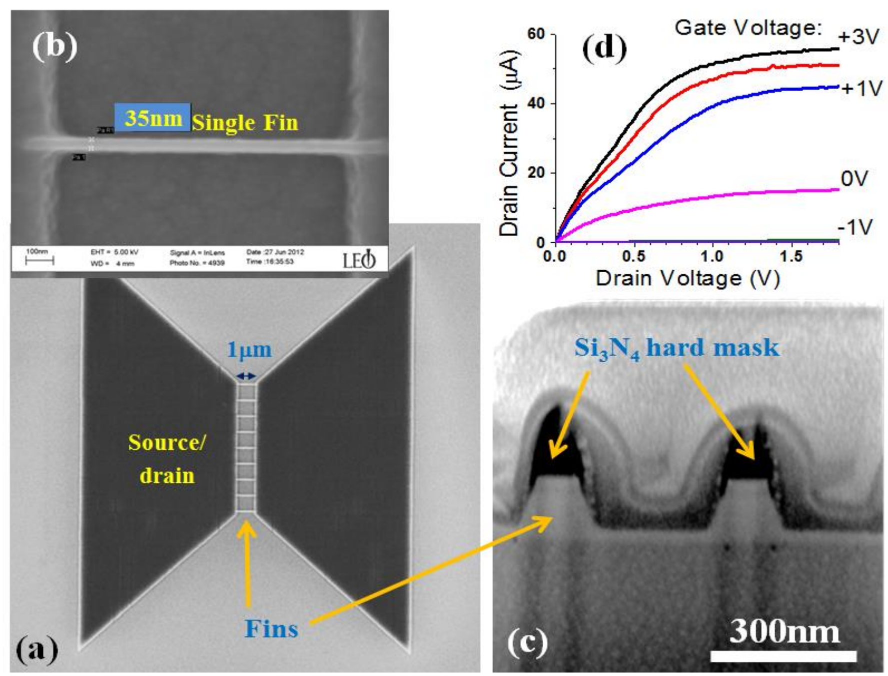
E-beam exposure using Vistec VB 300

- NEB and HSQ negative resists: Fin Width down to 50 nm

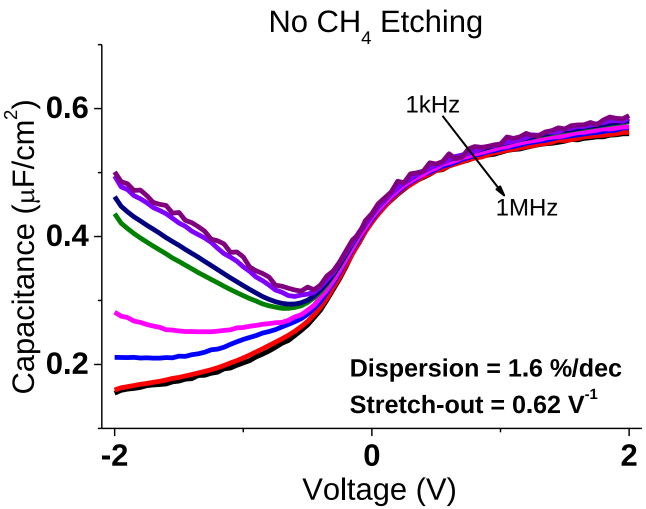
Plasma etching of hard mask pattern into InGaAs

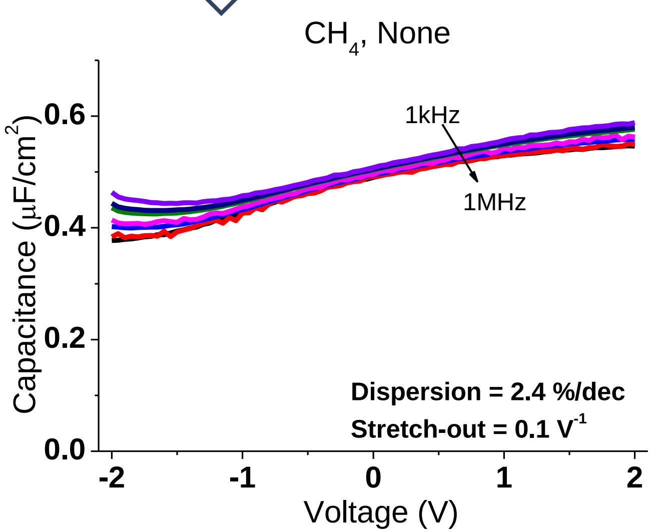
- $CH_4/H_2/Ar$ recipe optimized for smooth, vertical sidewalls
- Damage removal with diluted piranha wet etch





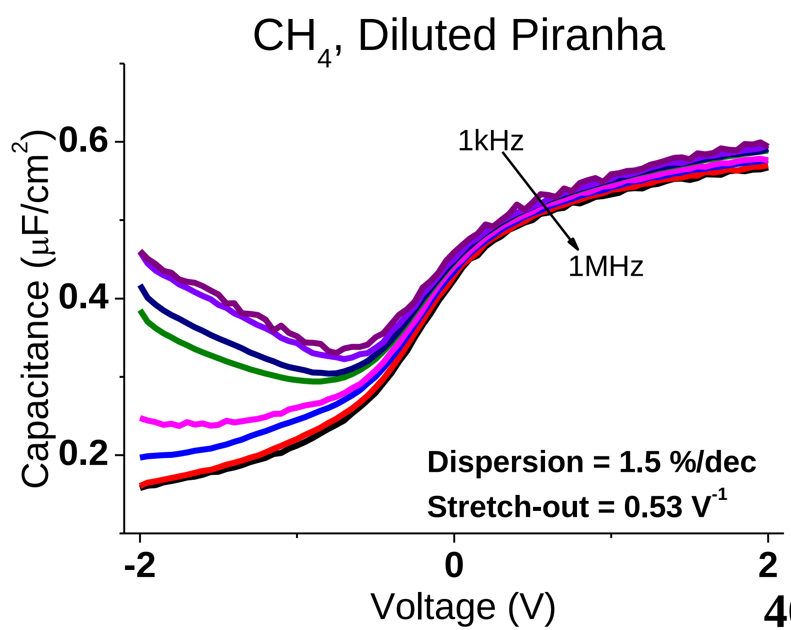
Ion Damage Removal



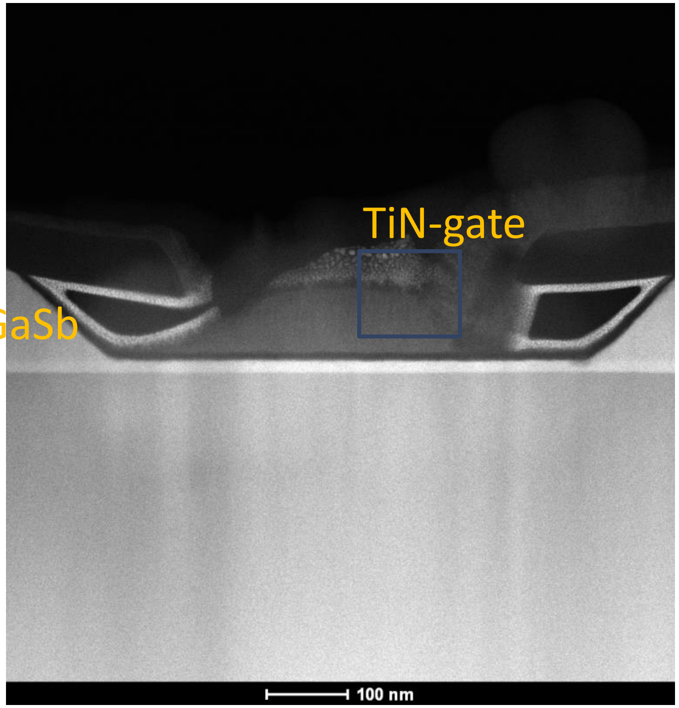


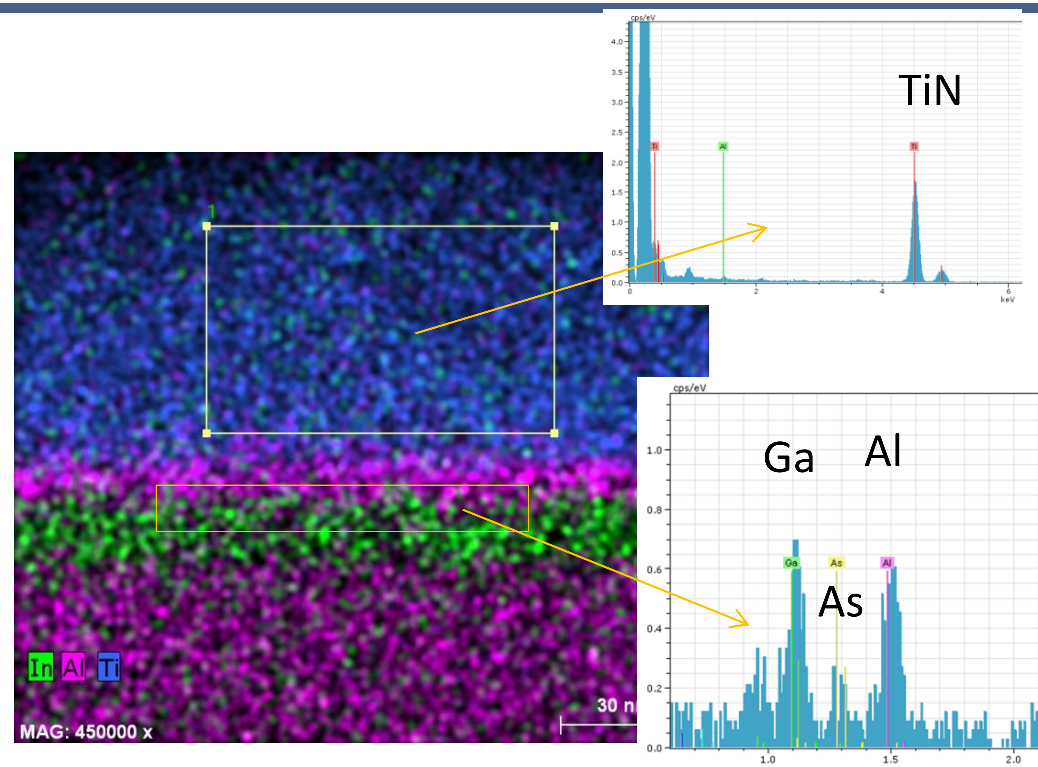
RIE damage removal after $CH_4/H_2/Ar$ etch

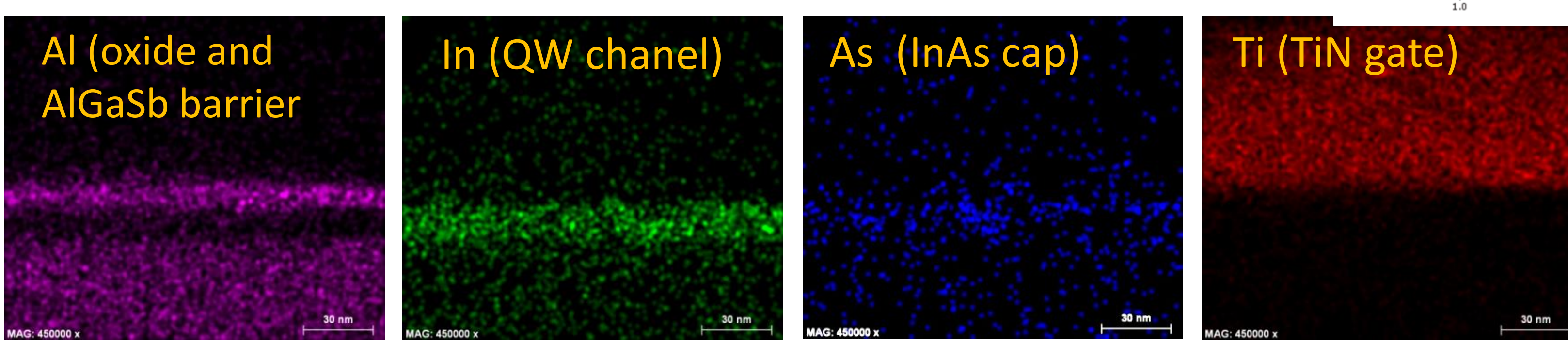
- **1µm n-$In_{0.53}$GaAs on n-GaAs MOS Capacitor**
- **Diluted Piranha = similar CV to as-grown surface**
- **CV characteristics restored**



STEM/EDX of gate-last MOSFET







- Gate-last flow MOSFET with epi p^{+}-GaSb SD and InAs etch stop layer
- After TMAH recess etch, InAs (1.5nm) is present on the surface

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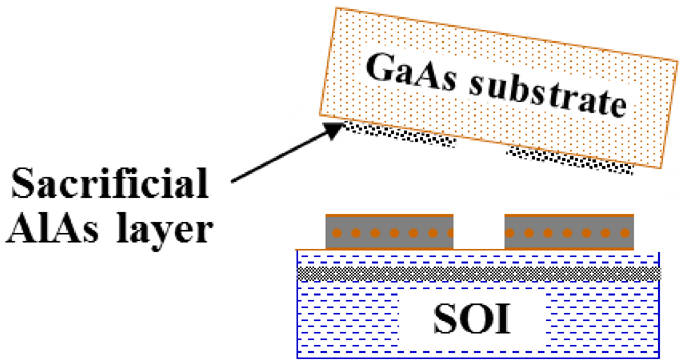
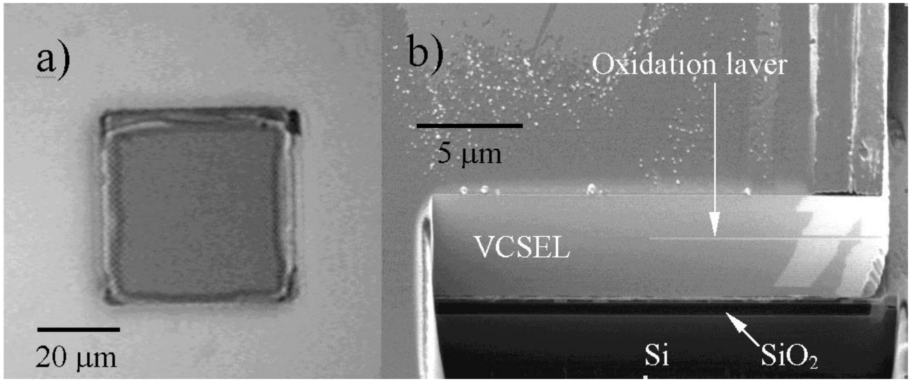
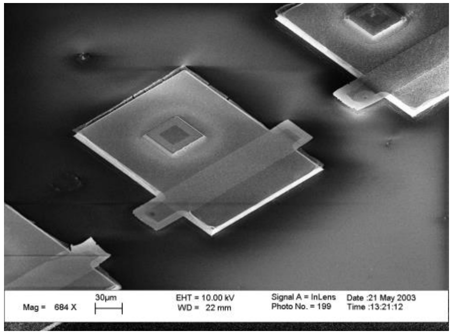
Oxidation Lift-off Technology

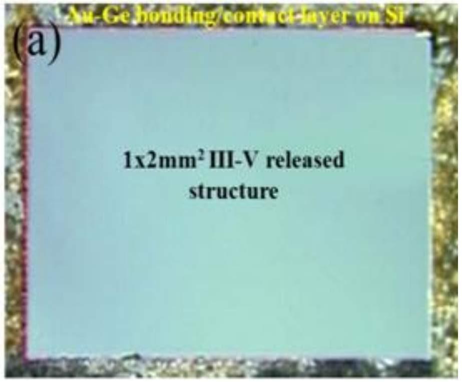
Oxidation lift-off

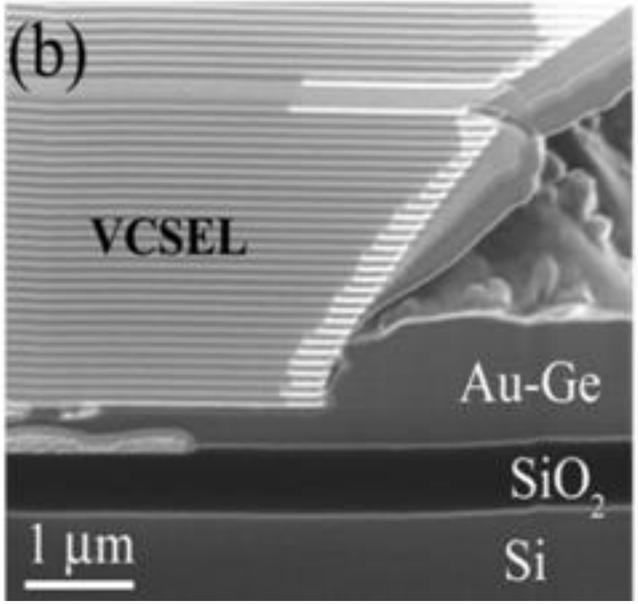


FIB cross-sections of the device fabricated by oxidation lift-off technique.









- Bonding by Au-Ge eutectic or polymer
- Bonding, device separation and formation of the oxide isolation I the same process

Conclusions

- Group III-V technologies are rapidly progressing towards mainstream logic ICs
- III-V materials have credible benefits for photodetectors:
  - High carrier velocity,
  - Low saturation field
- Planar lateral field architecture is beneficial for fast UV PD
  - Low capacitance
  - Transport close to the surface
  - Reduced volume for current
- Materials benefits + Available technologies => ps PDs ?

Acknowledgements

CNSE students

- Alex Varghese
- Rama Kambhampati (GF)
- Andrew Greene
- Shailesh Madisetti
- Thenappan Chidambaram

CNSE Staff

- Michael Yakimov
- Vadim Tokranov
- Shun Sasaki

Funding:

- NSF
- AFOSR
- SRC
- INTEL
- GLOBALFOUNDRIES

Academia collaborators

- Peide Ye (Purdue)
- Jesus del Alamo (MIT)
- Jack Lee (UTexas at Austin)
- Darrel Schlom (Cornell)
- Nikolai Faleev (Arizona State)

Industrial collaborators

- Sergei Koveshnikov (Intel)
- Dmitry Veksler (Sematech)
- Niti Goel (Intel)
- Ajey Jacob (GF)
- Steven Bentley (GF)

Many thanks to FNAL

- Pavel Murat
- Erik Ramberg